

Compal Confidential

NCWGO/H0 Schematics Document

AMD S1g1 / RS780MN/ SB710

2009 / 06 / 24

LA-5481

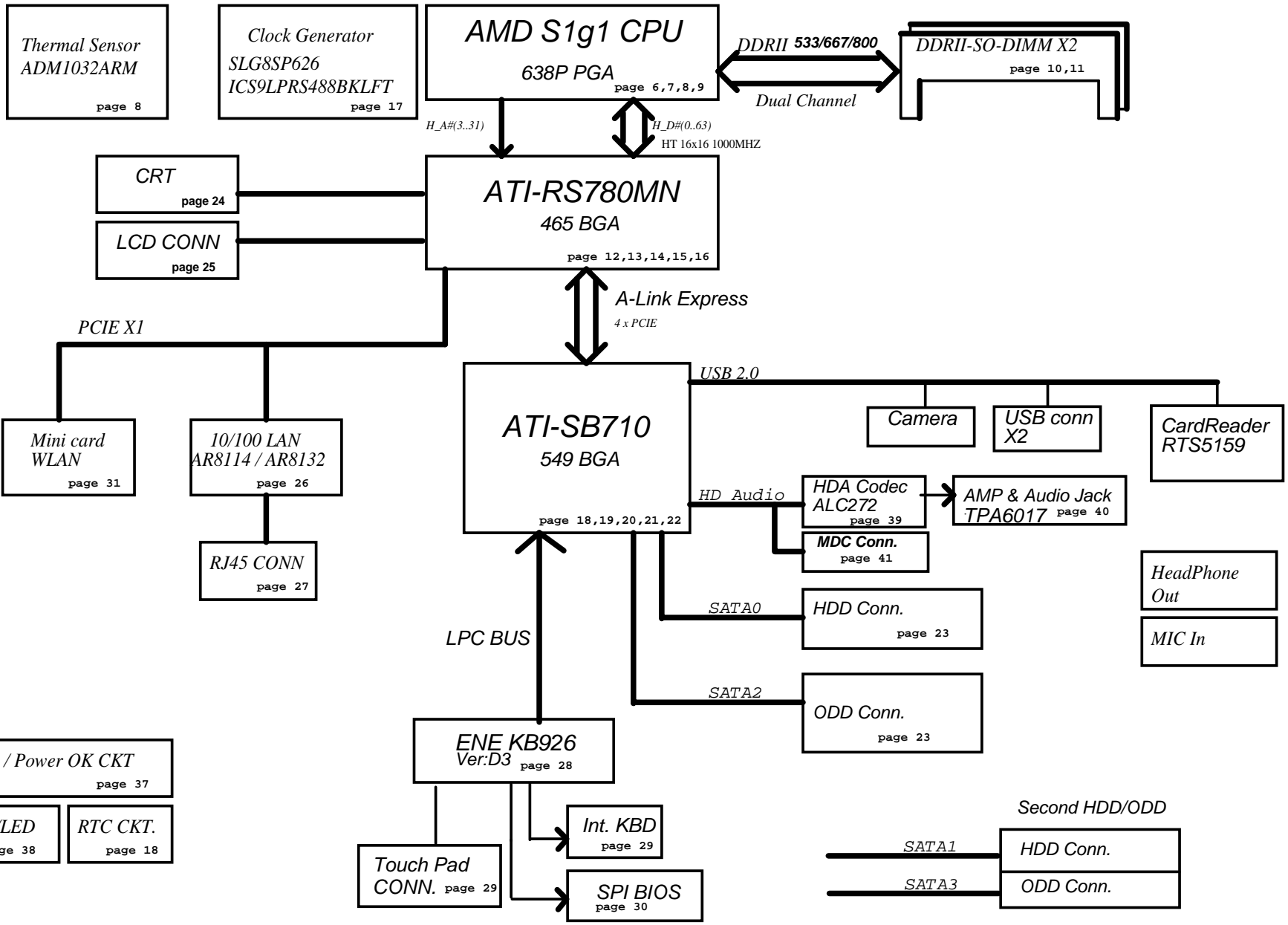
Rev:1.0

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				Custom	401743	C
				Date	Wednesday, June 24, 2009	Sheet 1 of 47

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Project Code: NCWG0/H0

File Name : LA-5481P



Power On/Off CKT / LID switch / Power OK CKT page 37

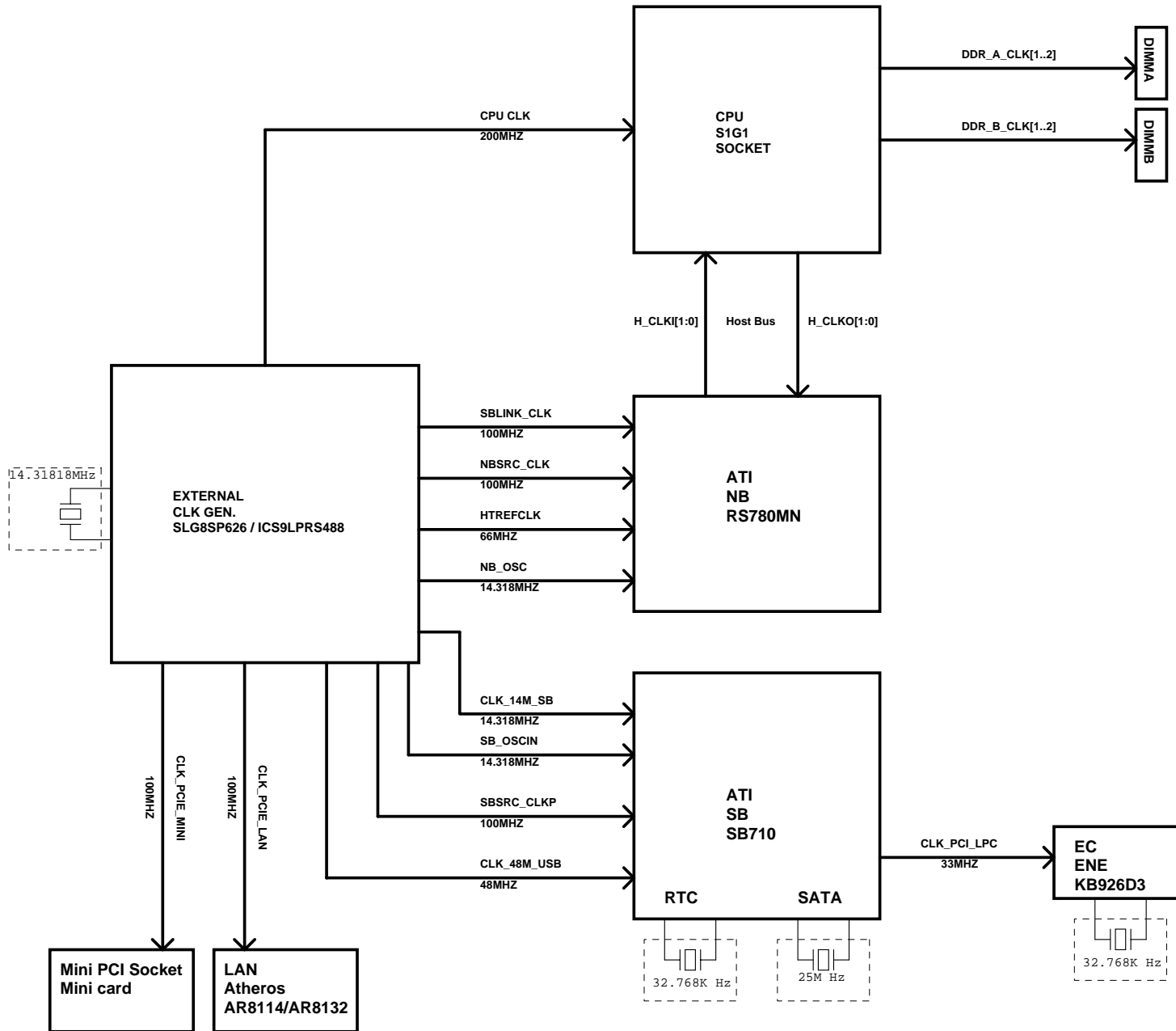
DC/DC Interface CKT. page 41

CIR/LED page 38

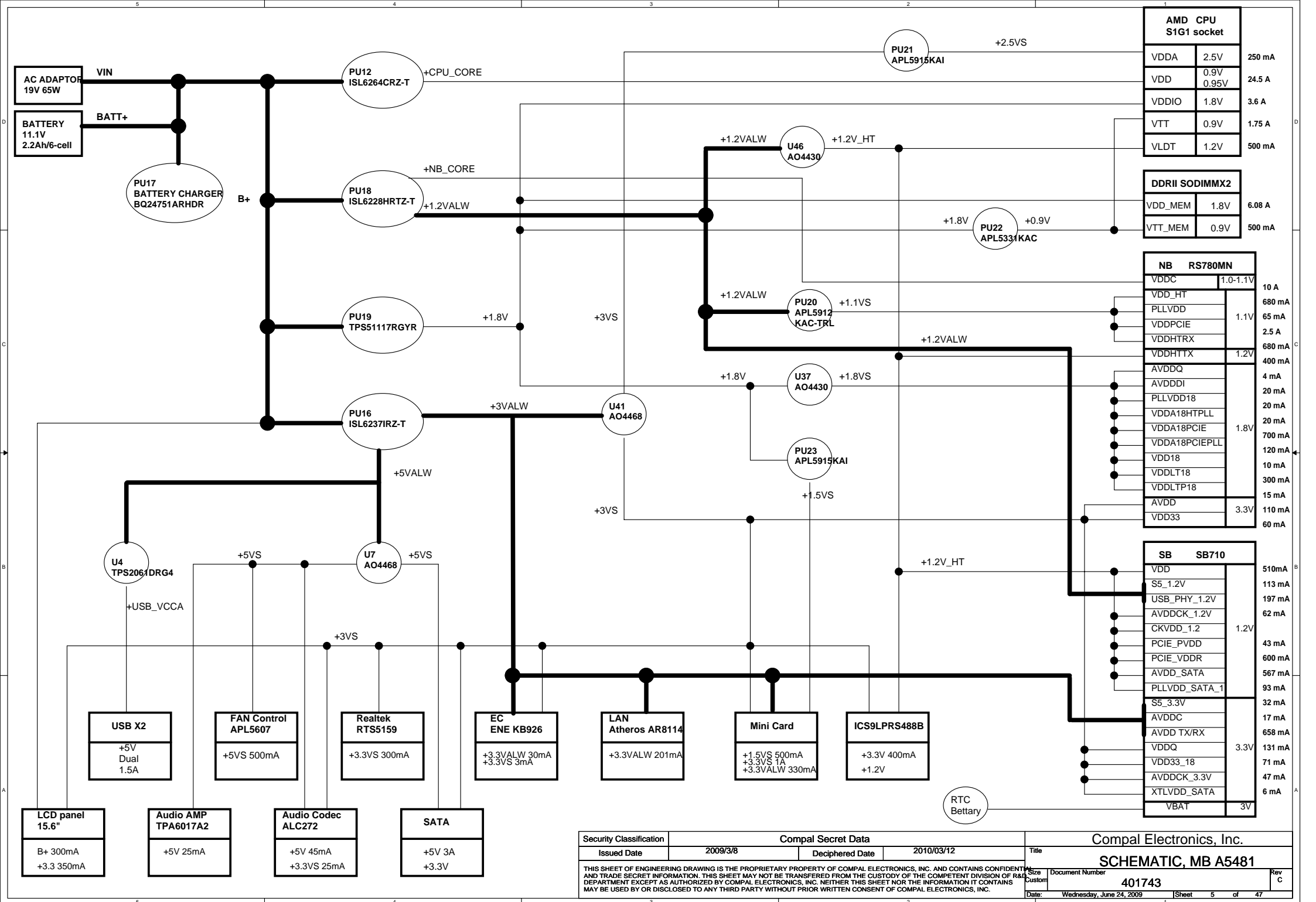
RTC CKT. page 18

Power Circuit DC/DC page 42~48

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				Custom	401743	C
				Date:	Wednesday, June 24, 2009	Sheet 2 of 47



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				Customer	401743
				Date:	Wednesday, June 24, 2009
				Sheet	4 of 47
				Rev	C



AMD CPU S1G1 socket		
VDDA	2.5V	250 mA
VDD	0.9V / 0.95V	24.5 A
VDDIO	1.8V	3.6 A
VTT	0.9V	1.75 A
VLDT	1.2V	500 mA

DDRII SODIMMx2		
VDD_MEM	1.8V	6.08 A
VTT_MEM	0.9V	500 mA

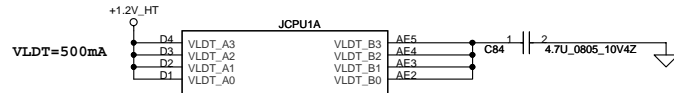
NB RS780MN		
VDDC	1.0-1.1V	10 A
VDD_HT		680 mA
PLLVDD	1.1V	2.5 A
VDDPCIE		65 mA
VDDHTRX		2.5 A
VDDHTX	1.2V	680 mA
AVDDQ		400 mA
AVDDI		4 mA
PLLVDD18		20 mA
VDDA18HTPLL	1.8V	20 mA
VDDA18PCIE		700 mA
VDDA18PCIEPLL		120 mA
VDD18		10 mA
VDDLTP18		300 mA
AVDD		15 mA
VDD33	3.3V	110 mA
		60 mA

SB SB710		
VDD		510 mA
S5_1.2V		113 mA
USB_PHY_1.2V		197 mA
AVDDCK_1.2V	1.2V	62 mA
CKVDD_1.2		
PCIE_PVDD		43 mA
PCIE_VDDR		600 mA
AVDD_SATA		567 mA
PLLVDD_SATA_1		93 mA
S5_3.3V		32 mA
AVDDC		17 mA
AVDD TX/RX		658 mA
VDDQ	3.3V	131 mA
VDD33_18		71 mA
AVDDCK_3.3V		47 mA
XTLVDD_SATA		6 mA
VBAT	3V	

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Date:	Wednesday, June 24, 2009	Sheet	5	of	47

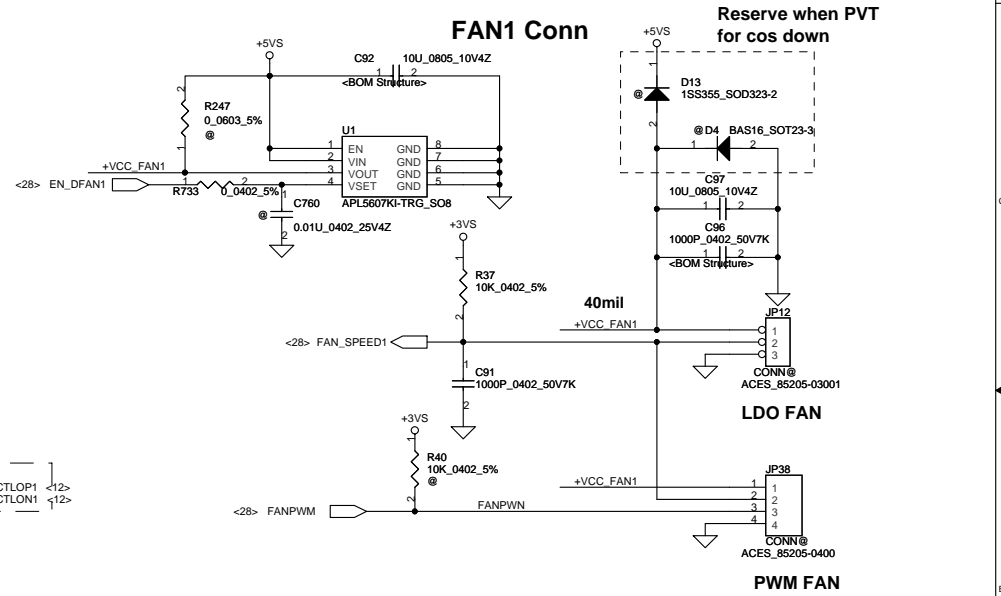
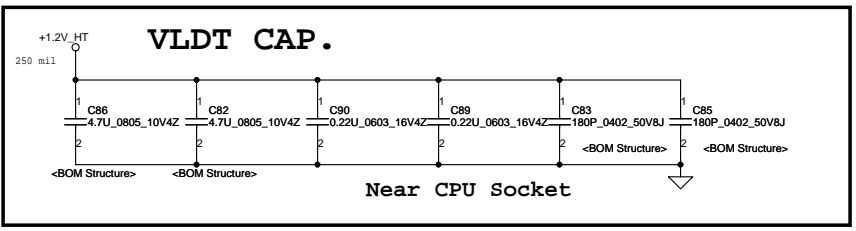
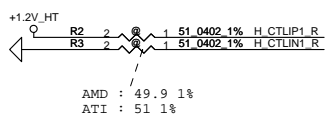
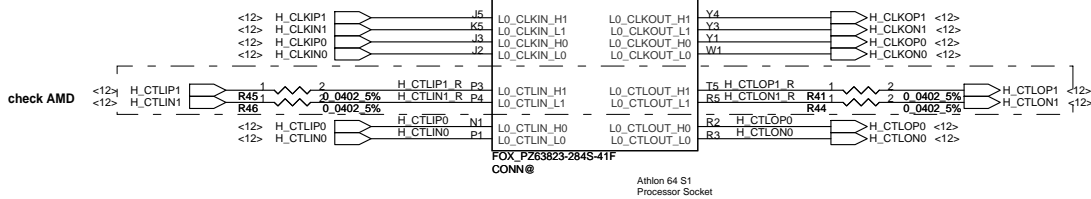
SCHEMATIC, MB A5481

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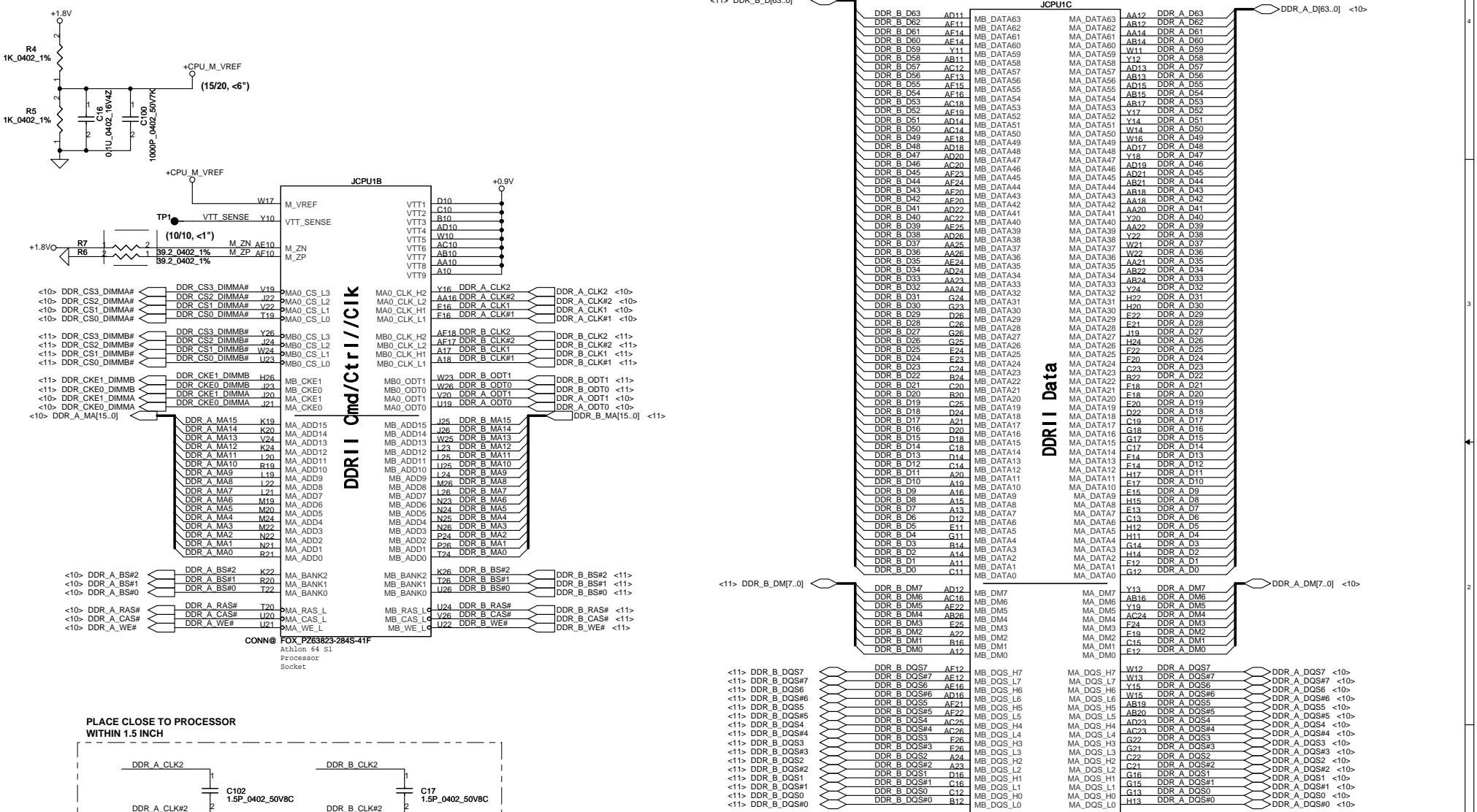
H_CADIP15 N5	L0_CADIN_H15	L0_CADOUT_H15	T4 H_CADOP15
H_CADIN15 P6	L0_CADIN_L15	L0_CADOUT_L15	T3 H_CADON15
H_CADIP14 M3	L0_CADIN_H14	L0_CADOUT_H14	V6 H_CADOP14
H_CADIN14 M4	L0_CADIN_L14	L0_CADOUT_L14	V5 H_CADON14
H_CADIP13 L5	L0_CADIN_H13	L0_CADOUT_H13	V3 H_CADOP13
H_CADIN13 M5	L0_CADIN_L13	L0_CADOUT_L13	V4 H_CADON13
H_CADIP12 K3	L0_CADIN_H12	L0_CADOUT_H12	V5 H_CADOP12
H_CADIN12 K4	L0_CADIN_L12	L0_CADOUT_L12	V6 H_CADON12
H_CADIP11 H3	L0_CADIN_H11	L0_CADOUT_H11	AB5 H_CADOP11
H_CADIN11 H4	L0_CADIN_L11	L0_CADOUT_L11	AB4 H_CADON11
H_CADIP10 G5	L0_CADIN_H10	L0_CADOUT_H10	AB3 H_CADOP10
H_CADIN10 G6	L0_CADIN_L10	L0_CADOUT_L10	AB2 H_CADON10
H_CADIP9 E3	L0_CADIN_H9	L0_CADOUT_H9	AD5 H_CADOP9
H_CADIN9 E4	L0_CADIN_L9	L0_CADOUT_L9	AD4 H_CADON9
H_CADIP8 F5	L0_CADIN_H8	L0_CADOUT_H8	AD3 H_CADOP8
H_CADIN8 F6	L0_CADIN_L8	L0_CADOUT_L8	AD2 H_CADON8
H_CADIP7 N3	L0_CADIN_H7	L0_CADOUT_H7	T1 H_CADOP7
H_CADIN7 N2	L0_CADIN_L7	L0_CADOUT_L7	R1 H_CADON7
H_CADIP6 L1	L0_CADIN_H6	L0_CADOUT_H6	U2 H_CADOP6
H_CADIN6 M1	L0_CADIN_L6	L0_CADOUT_L6	U3 H_CADON6
H_CADIP5 L3	L0_CADIN_H5	L0_CADOUT_H5	V1 H_CADOP5
H_CADIN5 L2	L0_CADIN_L5	L0_CADOUT_L5	U1 H_CADON5
H_CADIP4 J1	L0_CADIN_H4	L0_CADOUT_H4	W2 H_CADOP4
H_CADIN4 K1	L0_CADIN_L4	L0_CADOUT_L4	W3 H_CADON4
H_CADIP3 G1	L0_CADIN_H3	L0_CADOUT_H3	AA2 H_CADOP3
H_CADIN3 H1	L0_CADIN_L3	L0_CADOUT_L3	AA3 H_CADON3
H_CADIP2 G3	L0_CADIN_H2	L0_CADOUT_H2	AB1 H_CADOP2
H_CADIN2 G2	L0_CADIN_L2	L0_CADOUT_L2	AA1 H_CADON2
H_CADIP1 E1	L0_CADIN_H1	L0_CADOUT_H1	AC2 H_CADOP1
H_CADIN1 E2	L0_CADIN_L1	L0_CADOUT_L1	AC3 H_CADON1
H_CADIP0 E3	L0_CADIN_H0	L0_CADOUT_H0	AD1 H_CADOP0
H_CADIN0 E2	L0_CADIN_L0	L0_CADOUT_L0	AC1 H_CADON0

HIT Interface

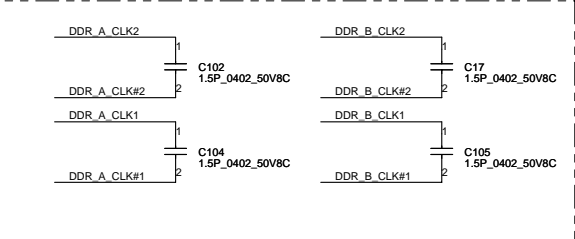


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				Sheet	6	of 46

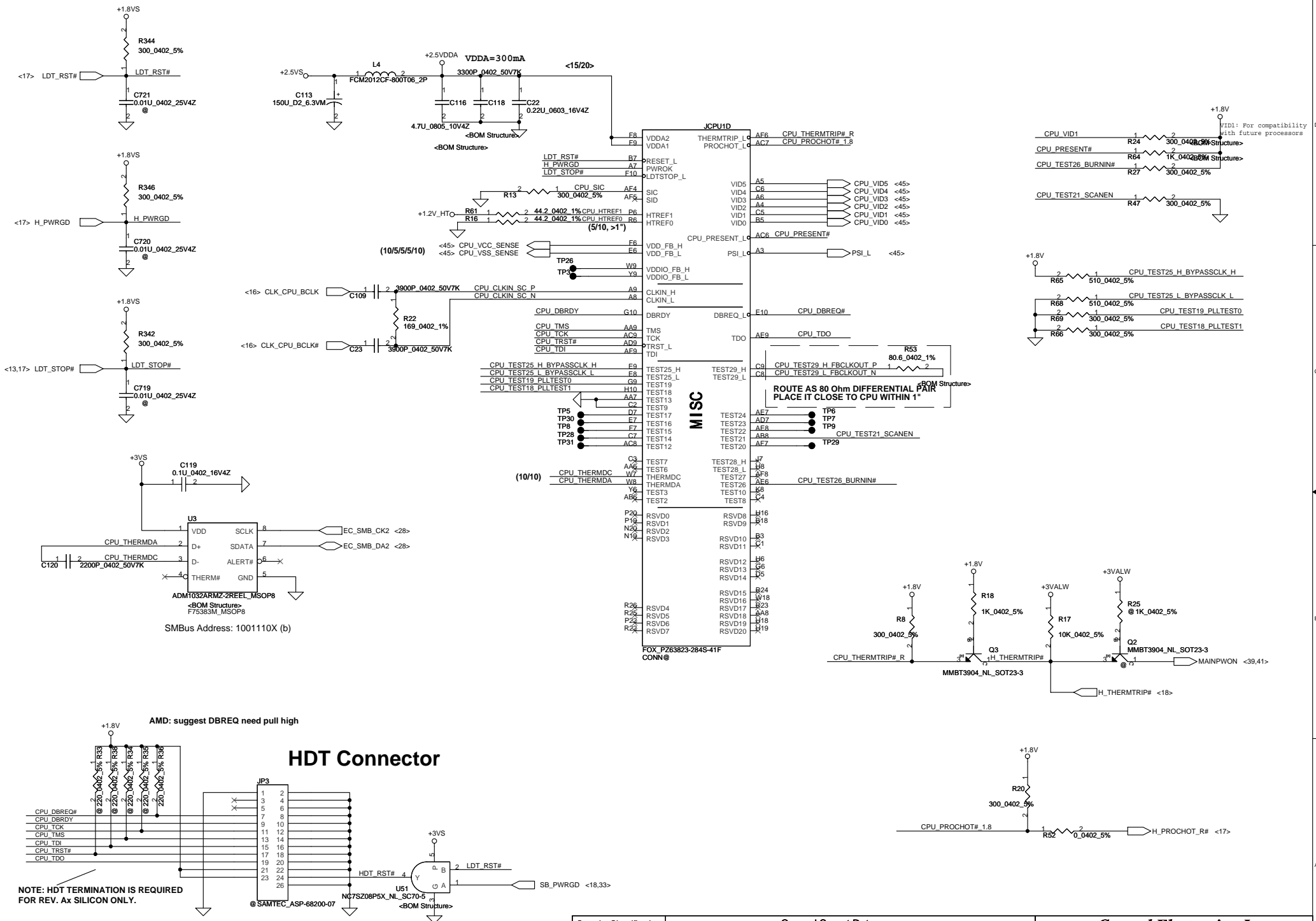
Processor DDR2 Memory Interface



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

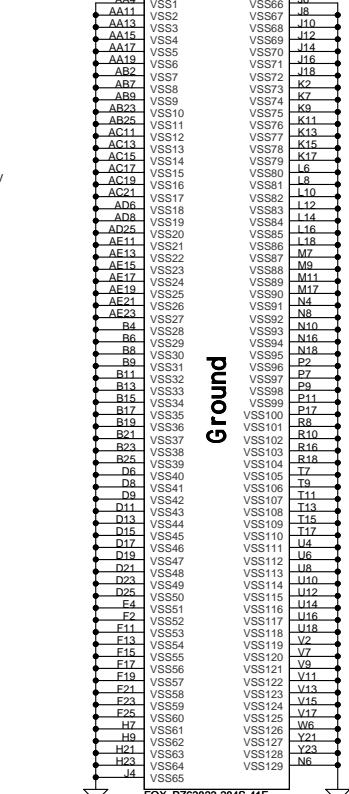
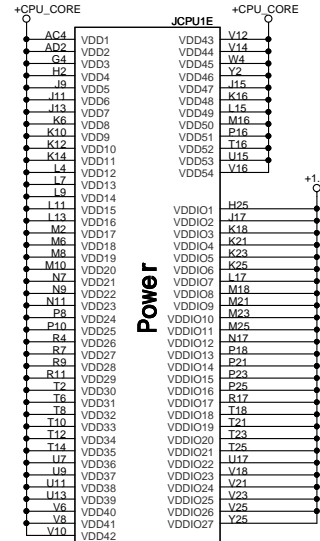
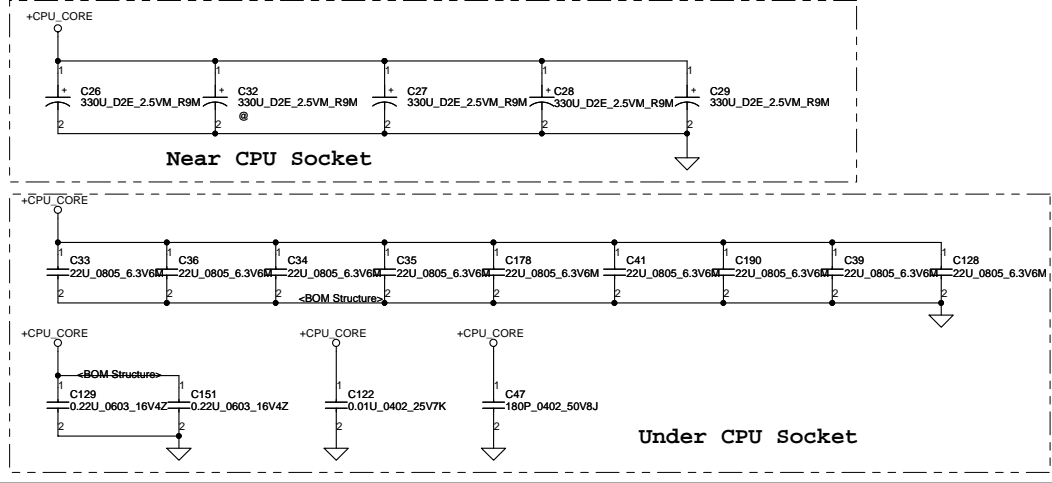


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Sheet	7	of	46		



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				401743	C
				Date: Wednesday, June 24, 2009	Sheet 8 of 46

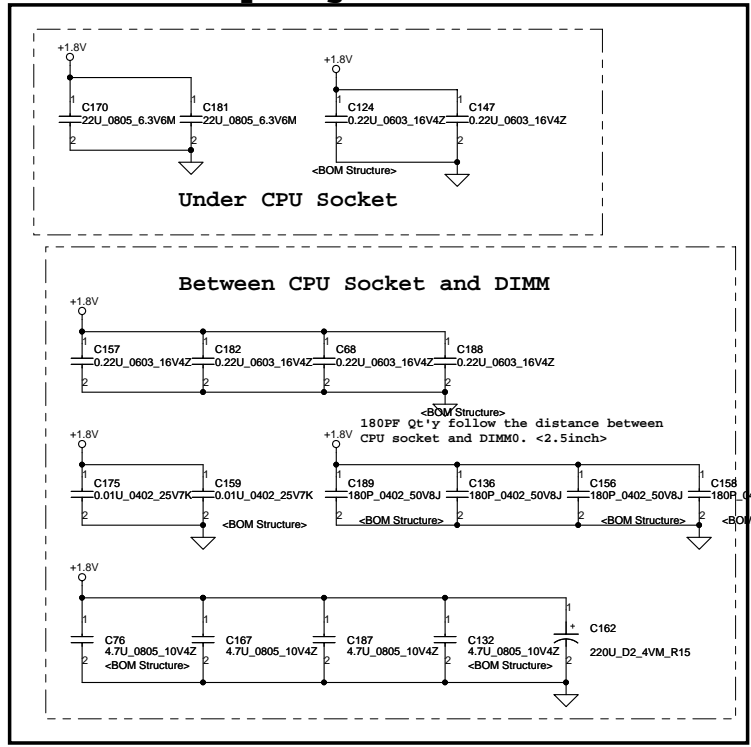
VDD(+CPU_CORE) decoupling.



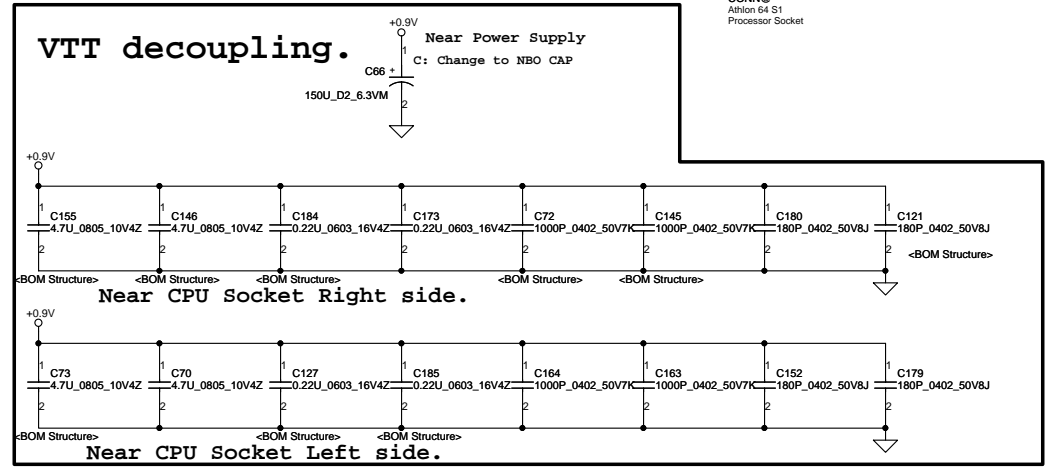
FOX_PZ63823-284S-41F
 CONN@
 Athlon 64 S1
 Processor Socket

FOX_PZ63823-284S-41F
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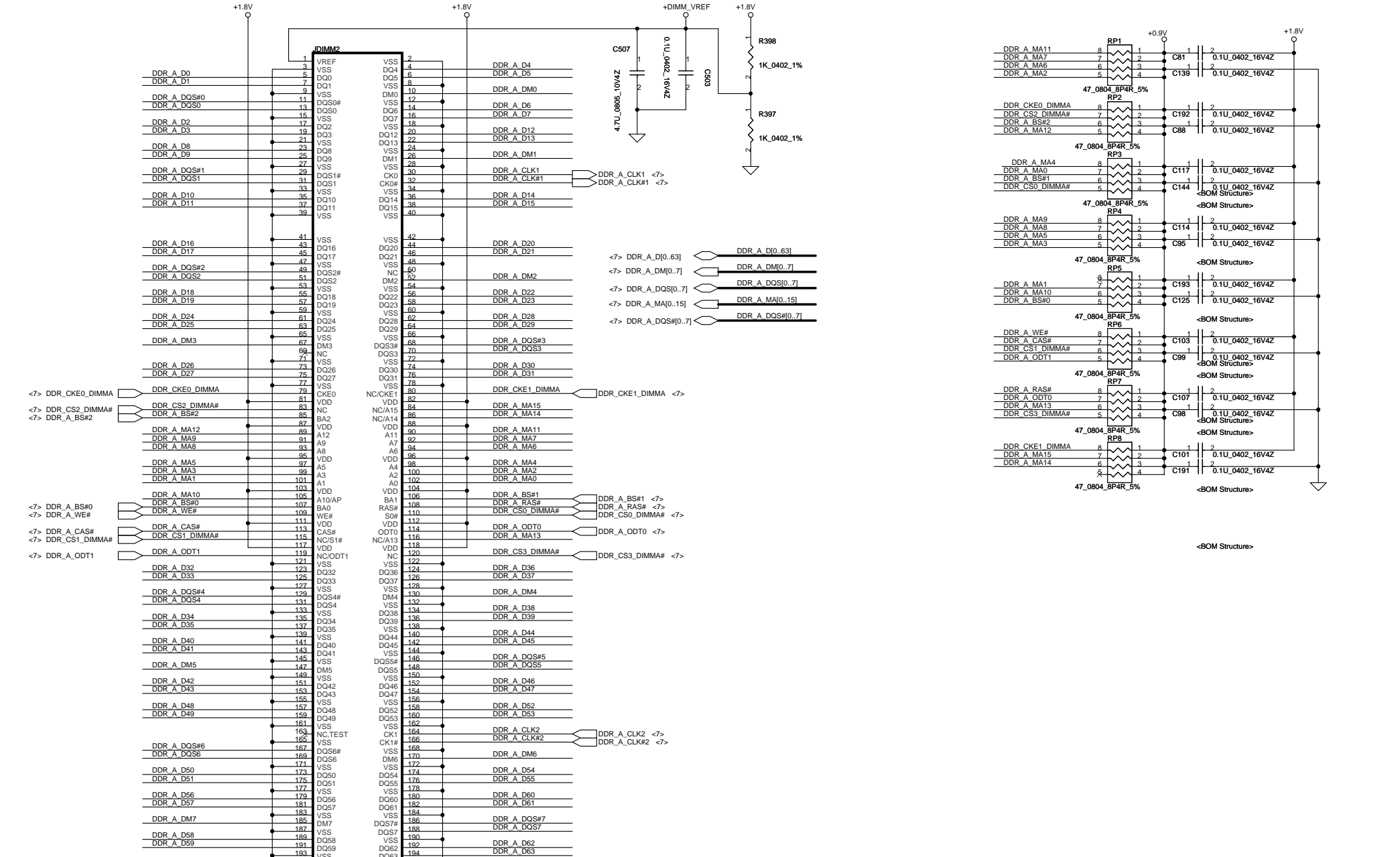
VDDIO decoupling.



VTT decoupling.



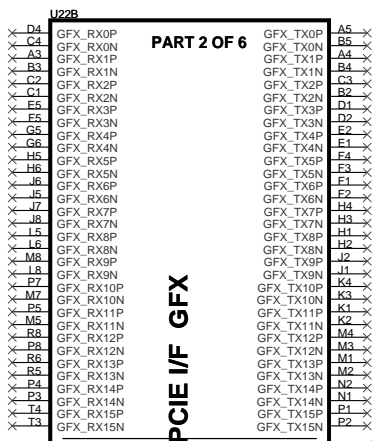
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				401743	Sheet 9 of 46	



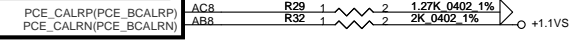
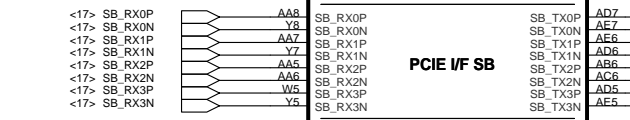
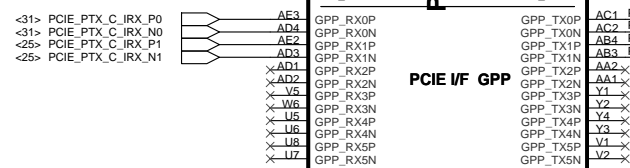
DIMM2 REV H:5.2mm (BOT)

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Title	401743
Document Number	401743
Date	Wednesday, June 24, 2009
Sheet	10 of 46



Check SW Routing
AN_RS780MN1. Only suggest pair0-3 can use for power save.

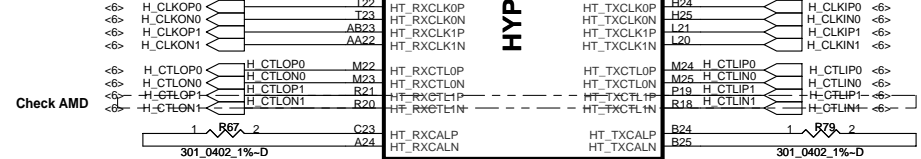


RS780M_FCBGA528
RS780MN-SA00002DR30 Ver:A13

RS780M Display Port Support (muxed on GFX)

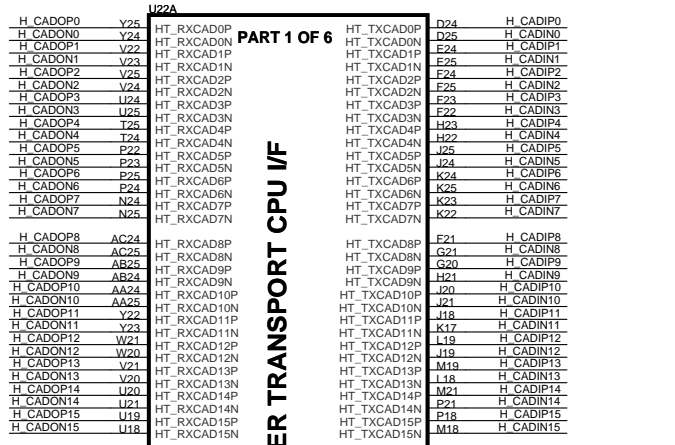
DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

HT Link
 When tune trace length, must keep 1:4 on self-trace

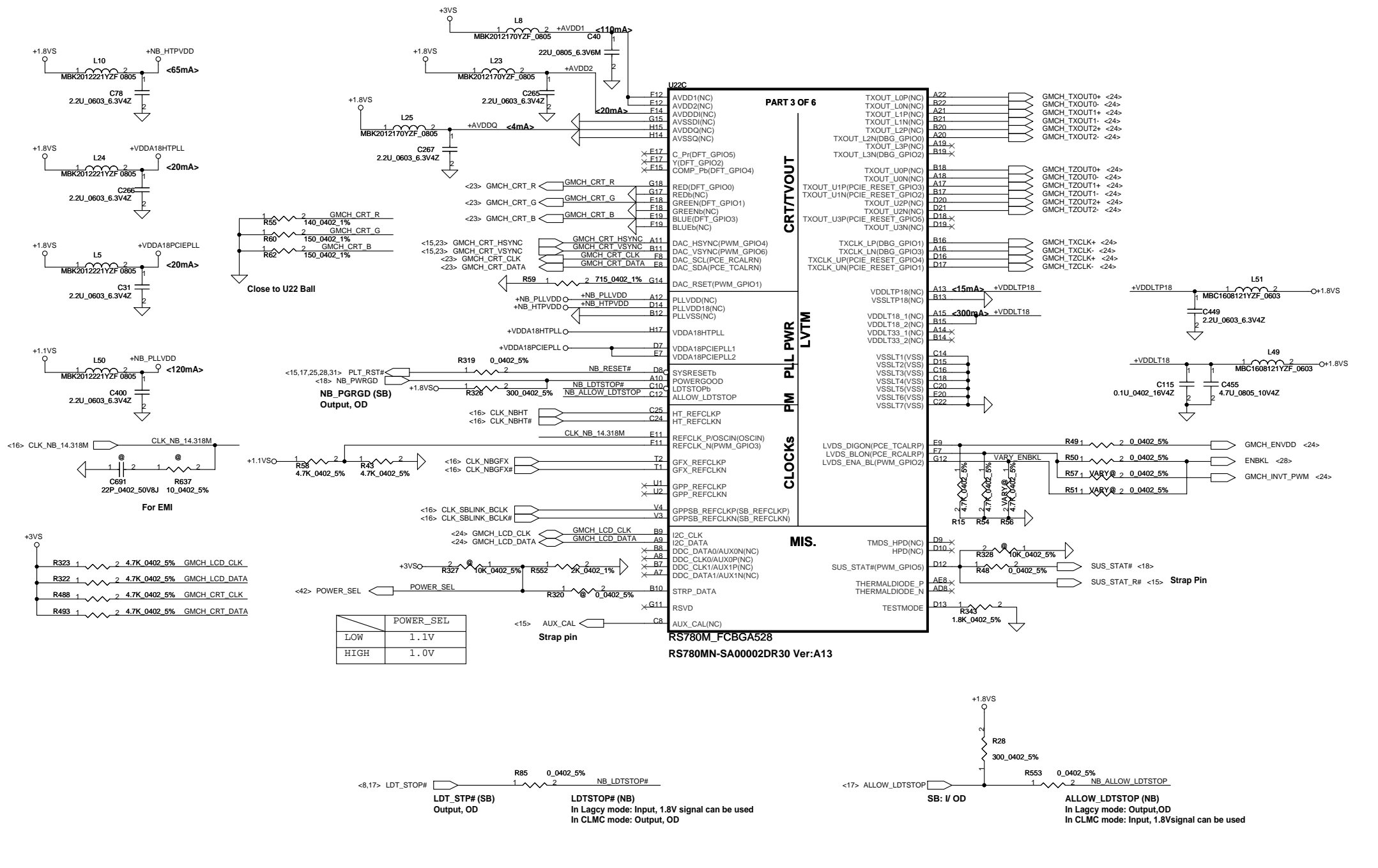


Place within 1" layout 4/8

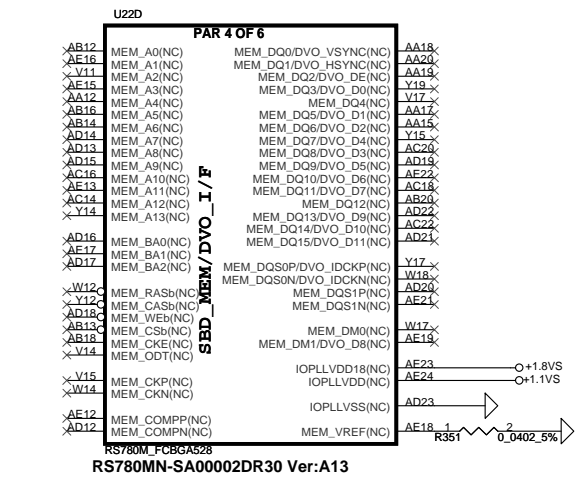
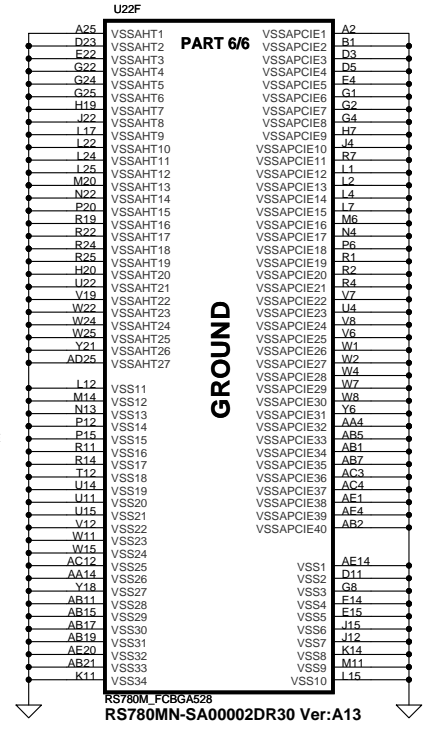
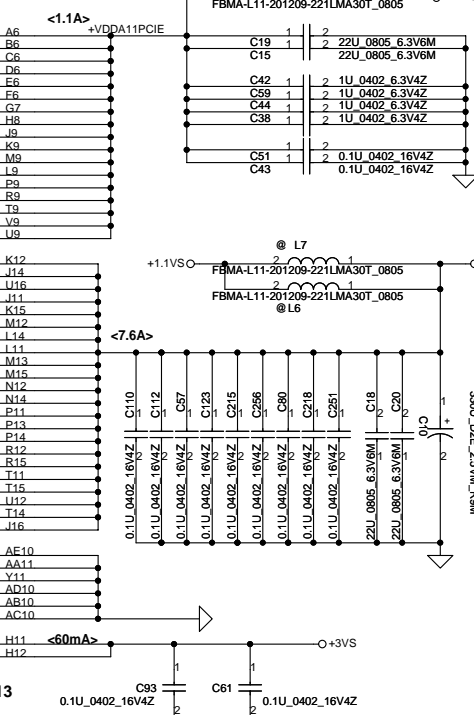
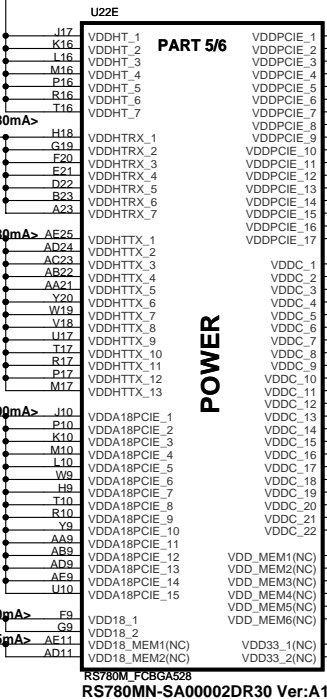
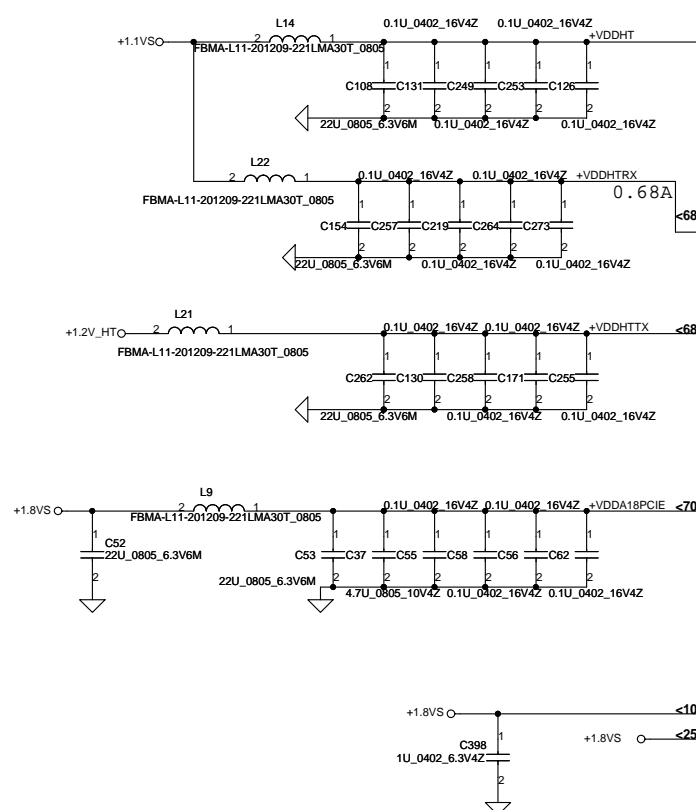
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Date:	Wednesday, June 24, 2009	Sheet	12	of 47	



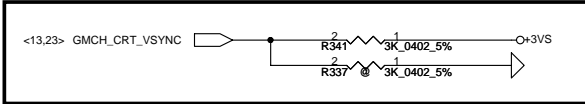
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				Document Number 401743
				Rev C
Date: Wednesday, June 24, 2009				Sheet 13 of 47



RS780M_FCBA528
RS780MN-SA00002DR30 Ver:A13

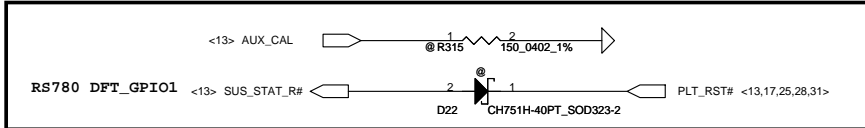
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RS780MN-SA00002DR30 Ver:A13

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Size	Customer	401743	Date:	Wednesday, June 24, 2009	Sheet 14 of 47



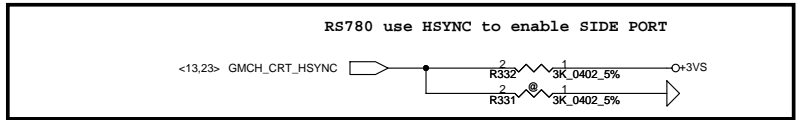
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
 1 : Disable (RS780)
 0 : Enable (Rs780)



DFT_GPIO1: LOAD_EEPROM_STRAPS

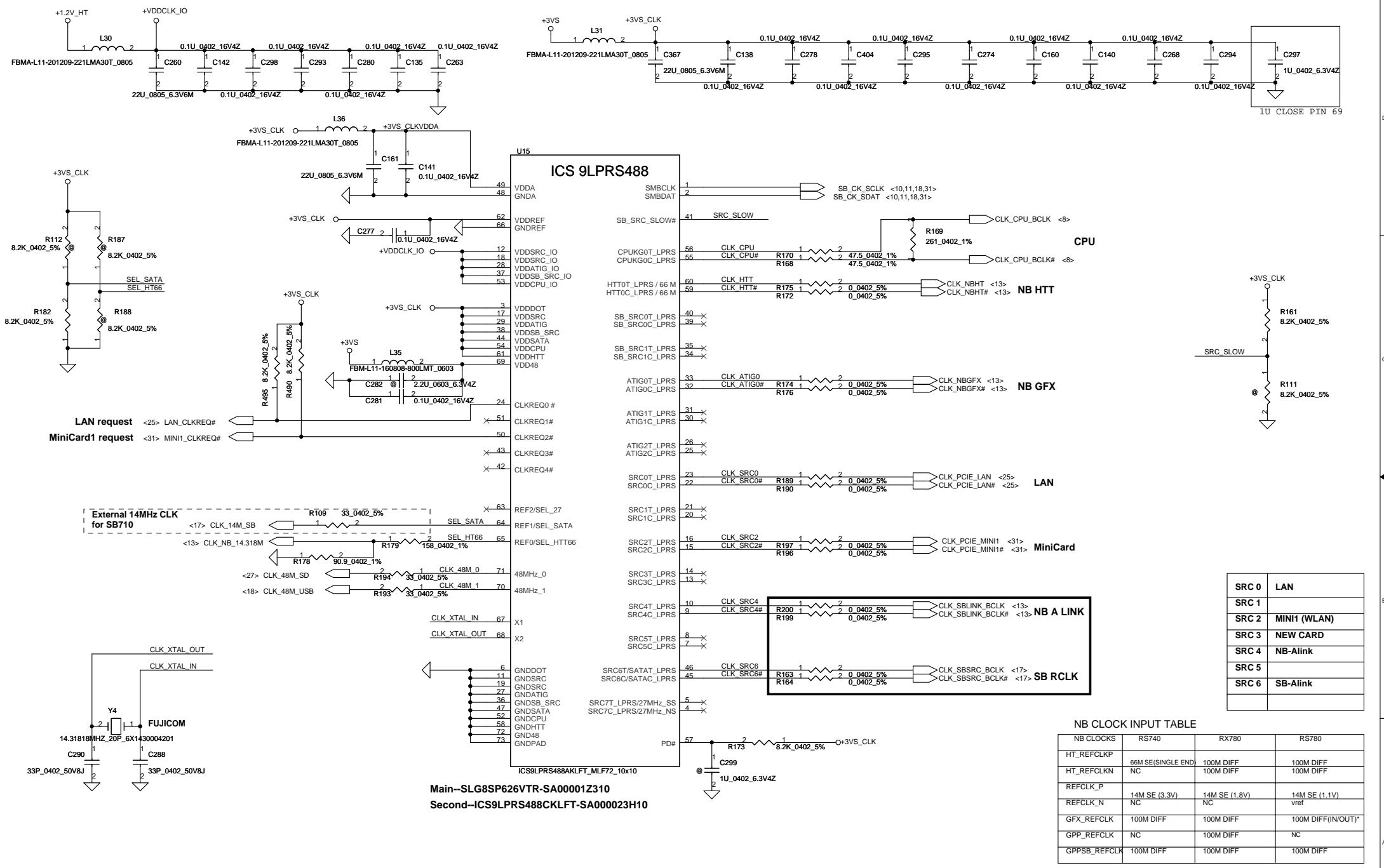
Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
 0. Enable (RS780)
 1 : Disable(RS780)

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Main-SLG8SP626VTR-SA00001Z310
 Second-ICS9LPRS488CKLFT-SA000023H10

SRC 0	LAN
SRC 1	
SRC 2	MINI1 (WLAN)
SRC 3	NEW CARD
SRC 4	NB-Alink
SRC 5	
SRC 6	SB-Alink

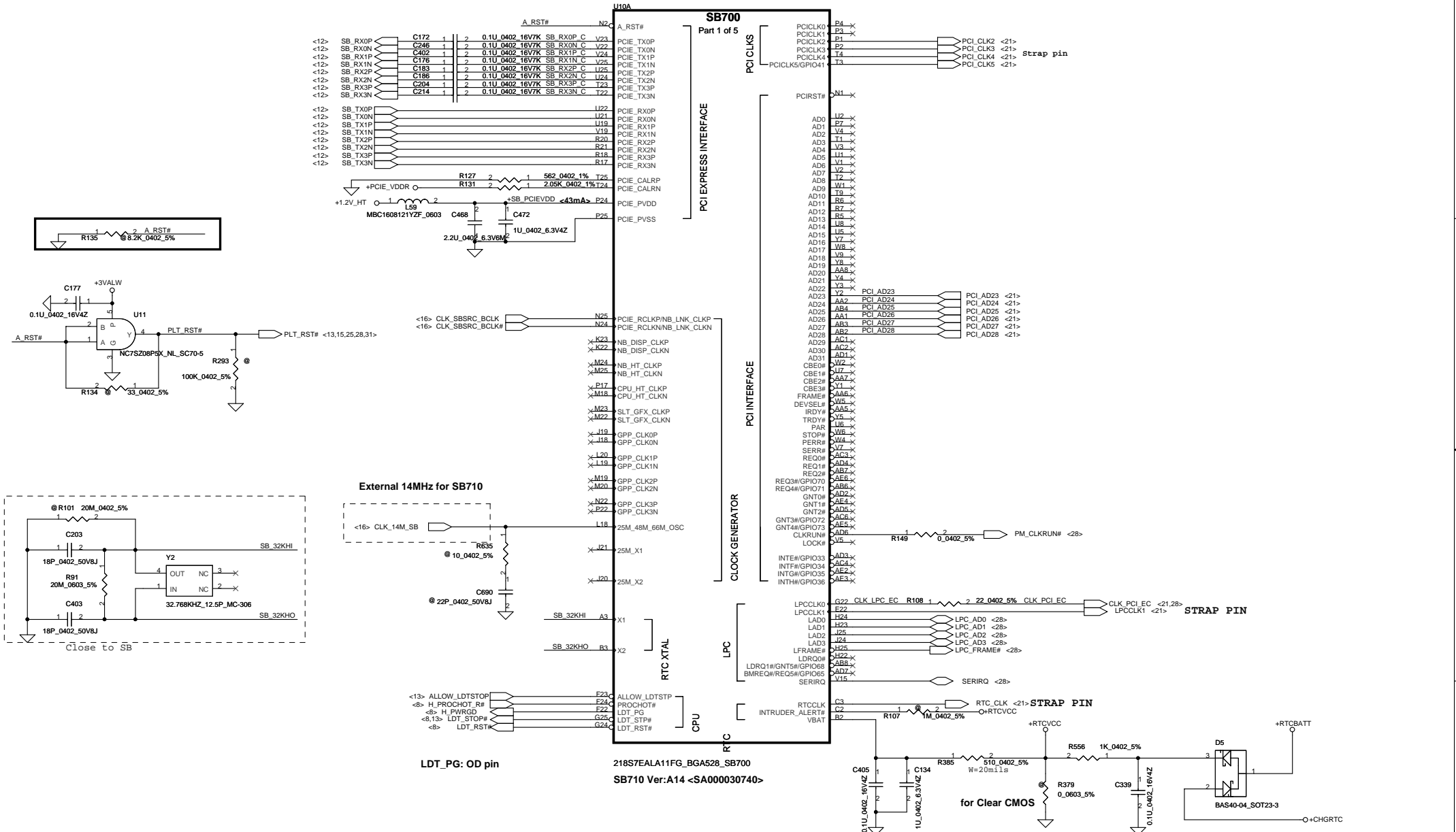
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	NC	NC	vref
REFCLK_N	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

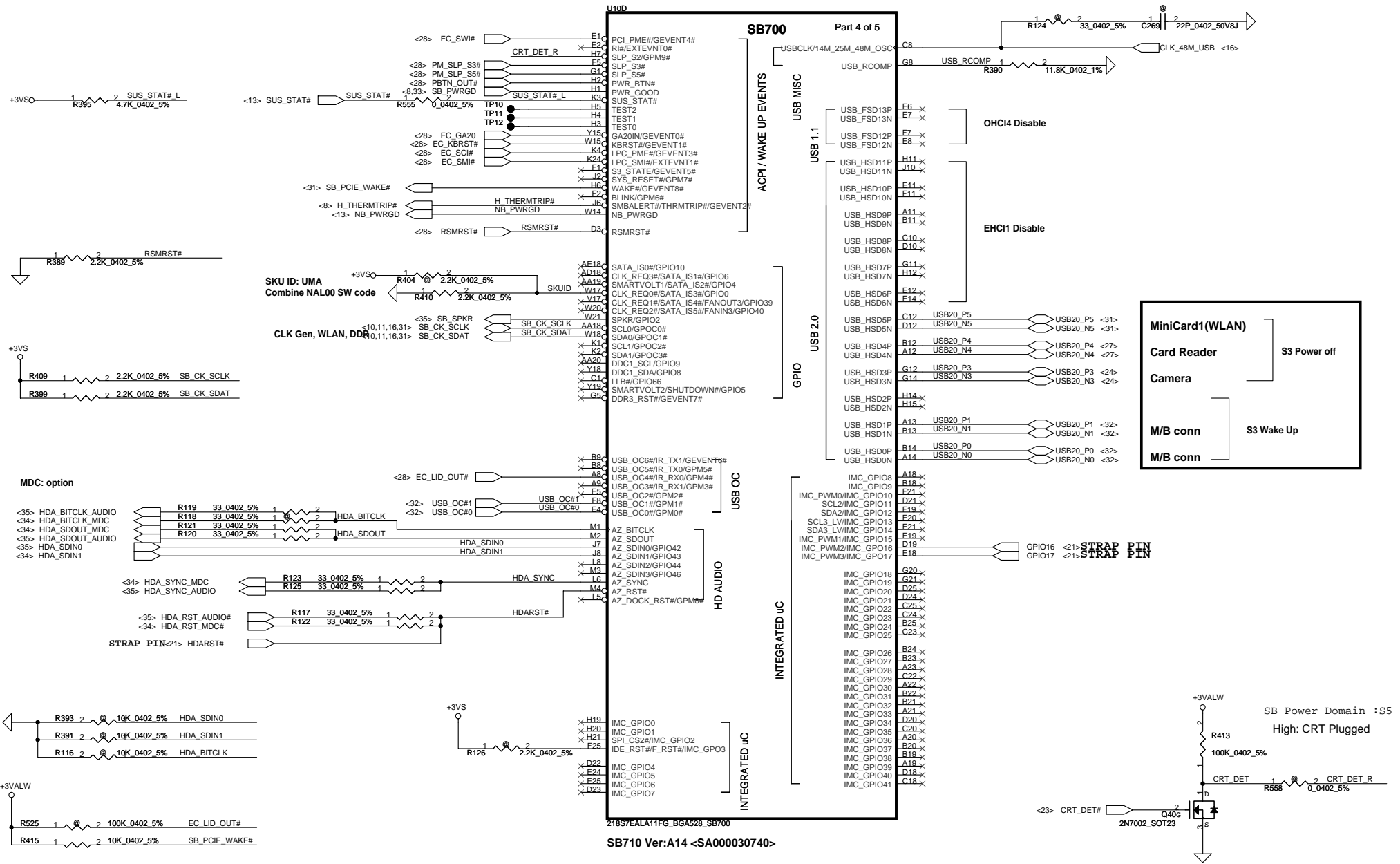
SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

SEL_27M	1	configure as 27M and 27M_SS output
No used	0	configure as SRC_7 output

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Size	Document Number	401743		Rev	C
Custom	Date: Wednesday, June 24, 2009		Sheet	16	of 47



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			Date: Wednesday, June 24, 2009 Sheet 17 of 47



SB710 Ver:A14 <SA000030740>

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				Customer	401743
				Date:	Wednesday, June 24, 2009
				Sheet	18 of 47

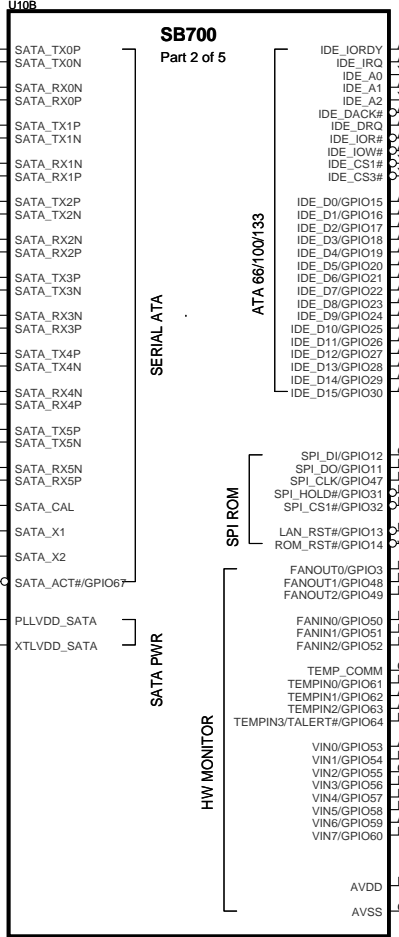
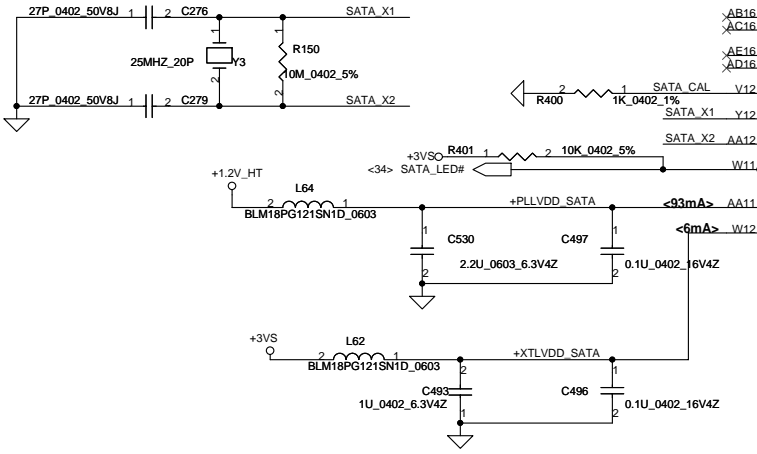
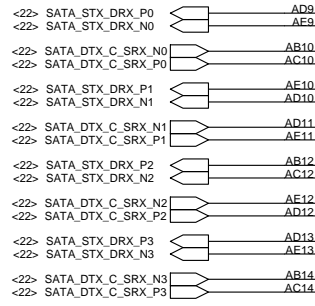
Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controller
Port 1	Secondary master	SATA controller
Port 2	Primary slave	SATA controller
Port 3	Secondary slave	SATA controller
Port 4	Primary (Secondary) master	PATA controller
Port 5	Primary (Secondary) slave	PATA controller

Main HDD

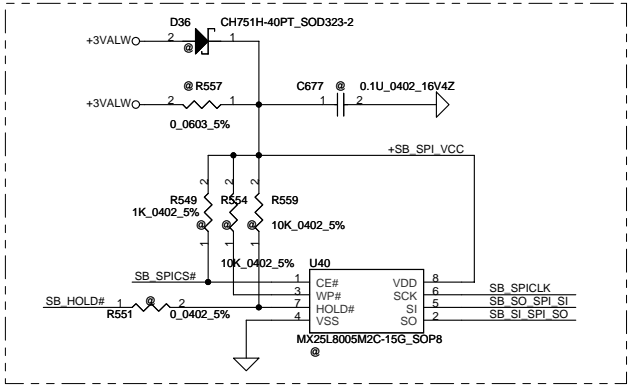
2nd HDD

Main ODD

2nd ODD



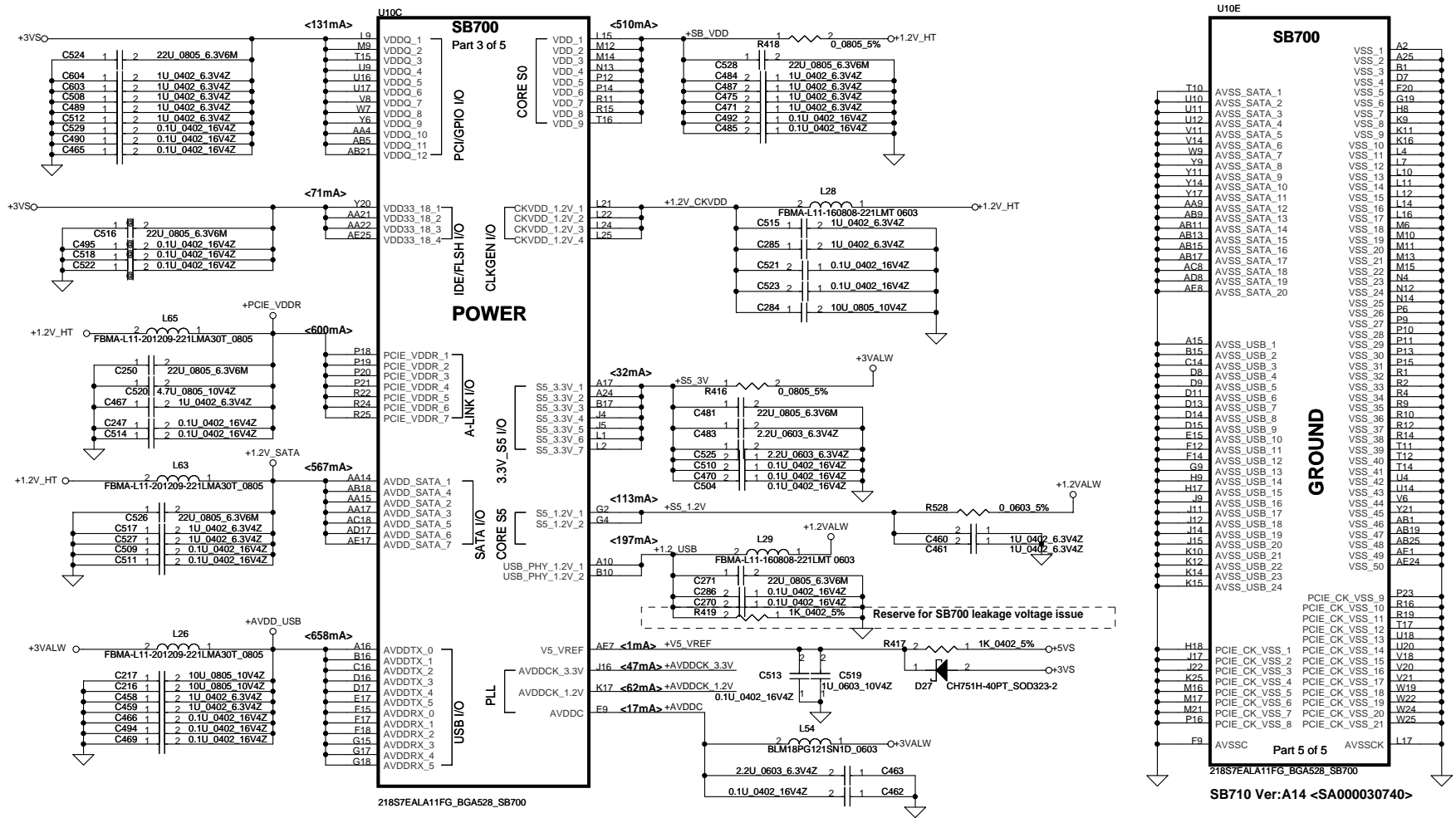
218S7EALA11FG_BGA528_SB700
SA00001S570 Ver:A12



Reserve For Debug

for ACIN level issue

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				401743	Rev C
Date:	Wednesday, June 24, 2009	Sheet	19	of 47	

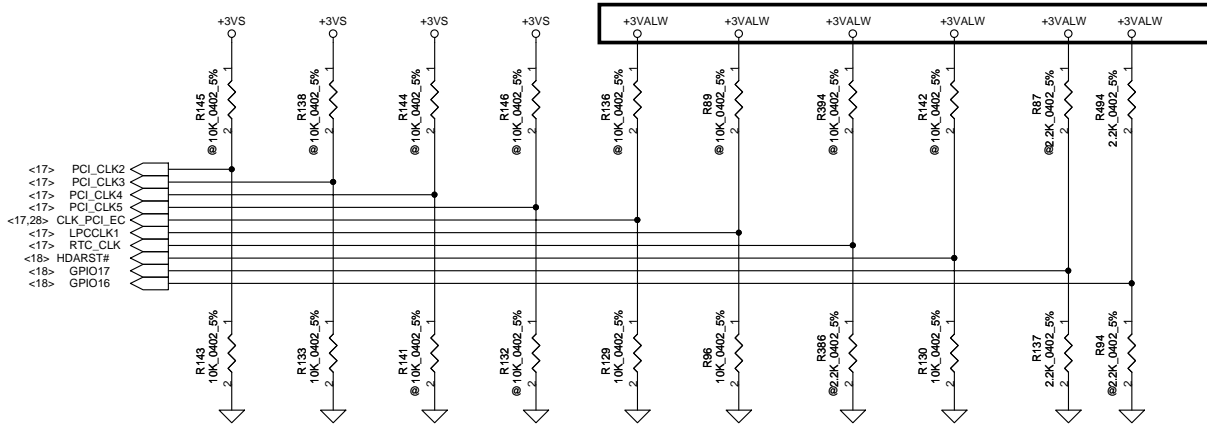


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Customer	401743		Date:	Wednesday, June 24, 2009	Sheet 20 of 47

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L,H = LPC ROM (Default L,NC) L,L = FWH ROM	

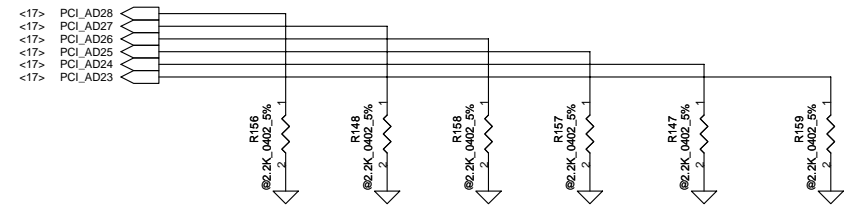


DEBUG STRAPS

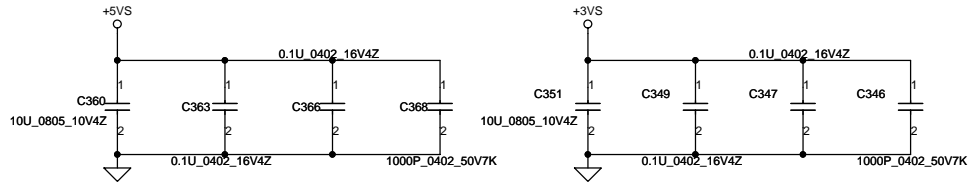
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

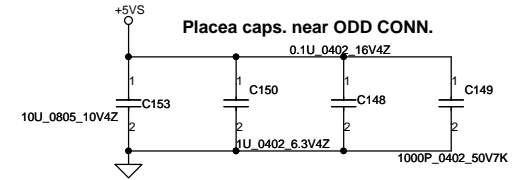
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



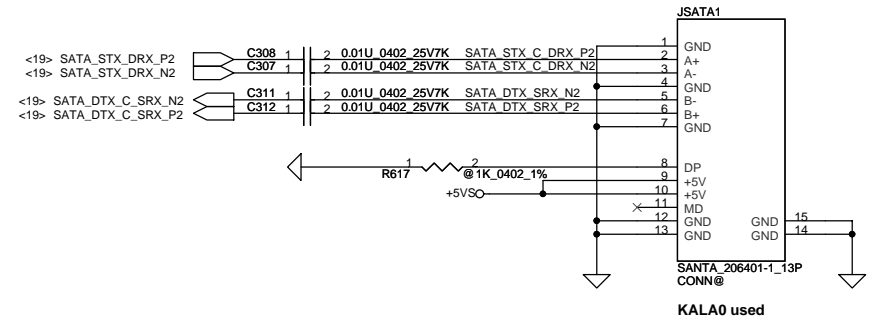
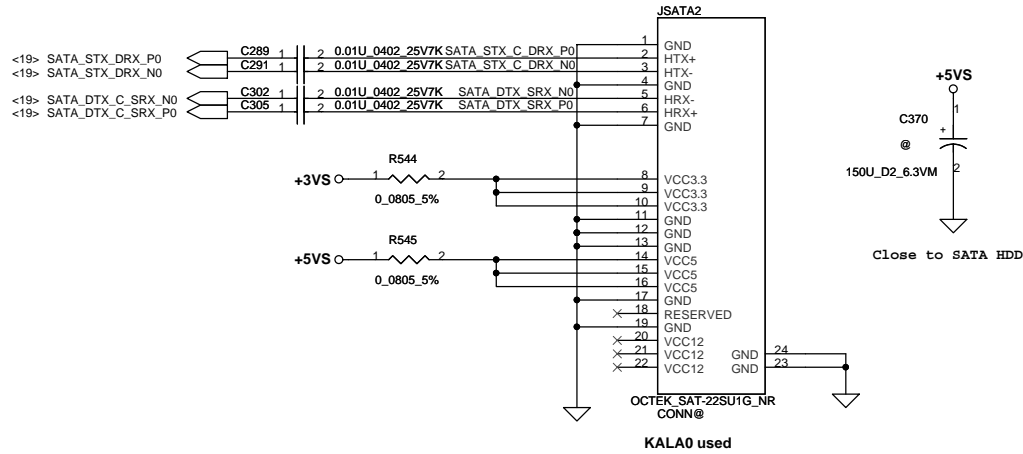
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Date:	Wednesday, June 24, 2009	Sheet	21	of	47



SATA HDD CONN

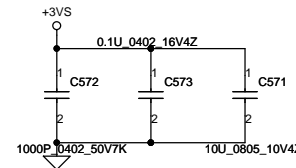
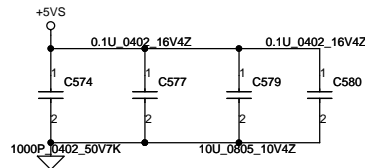
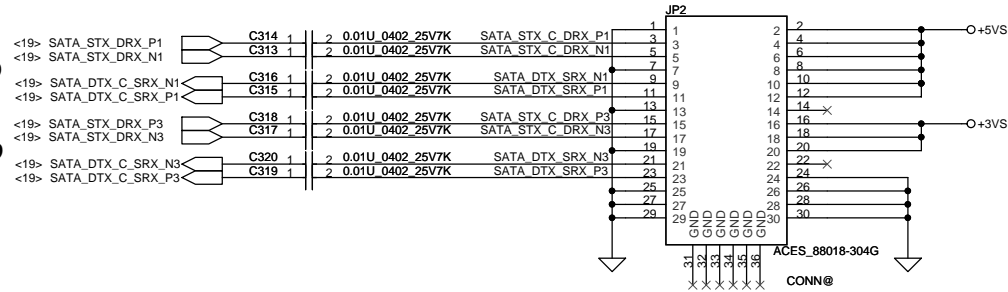


SATA ODD CONN



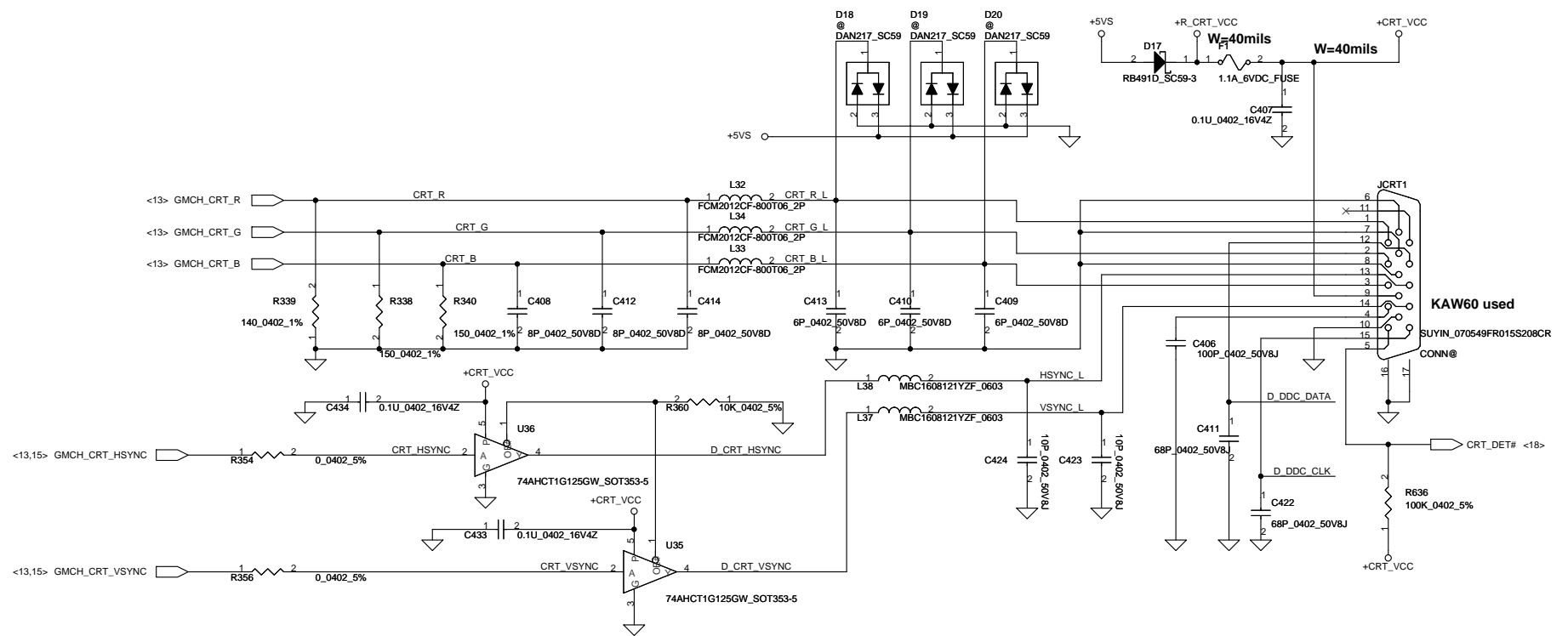
Second HDD

Second ODD

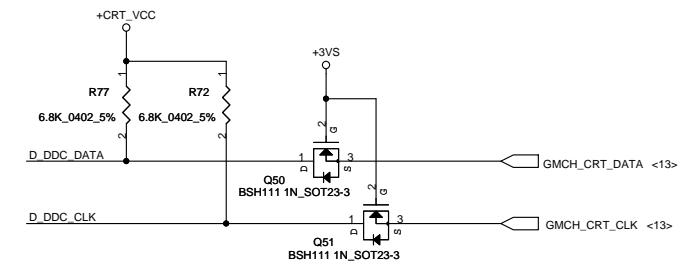


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				401743	Rev C
Date: Wednesday, June 24, 2009				Sheet	22 of 47

CRT Connector

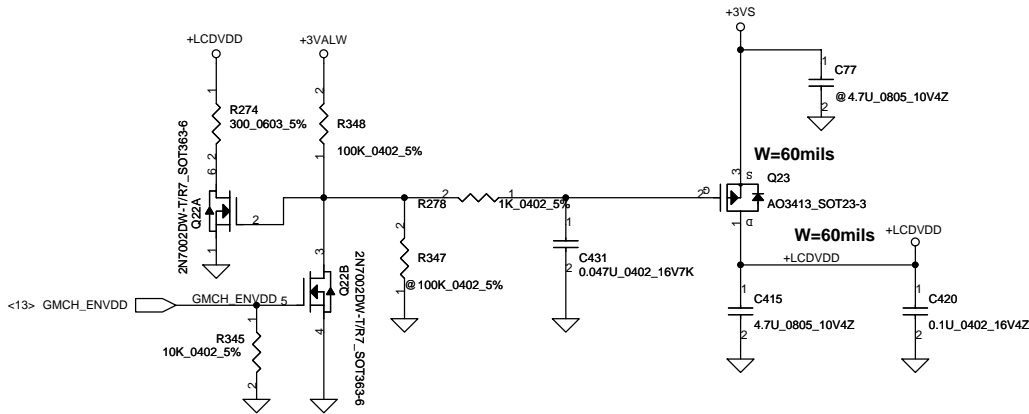


Close to Conn side

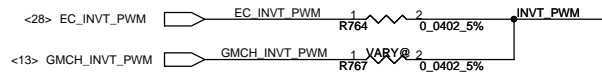
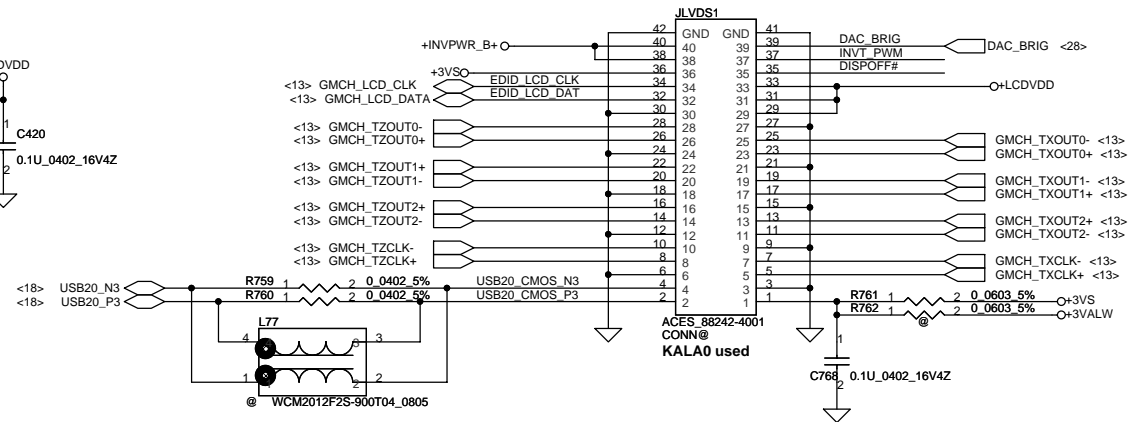


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				Rev C Sheet 23 of 47

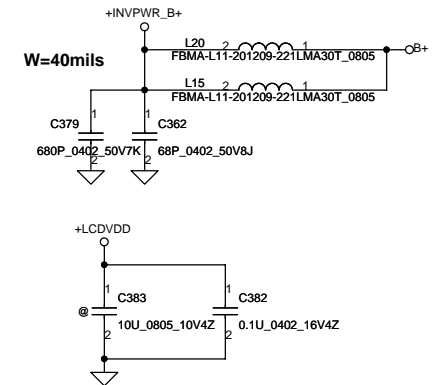
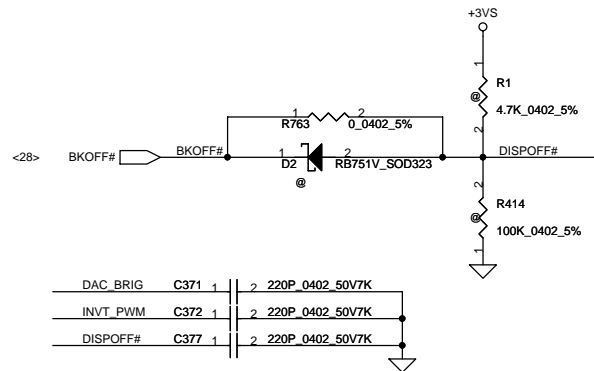
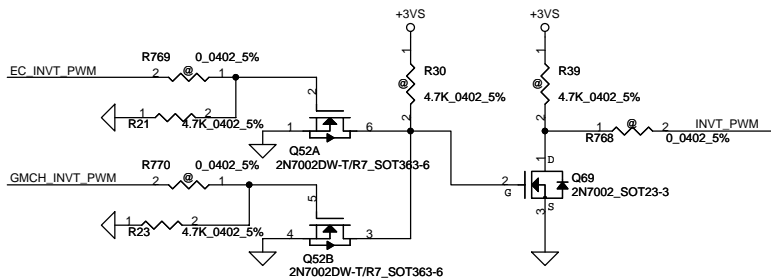
LCD POWER CIRCUIT



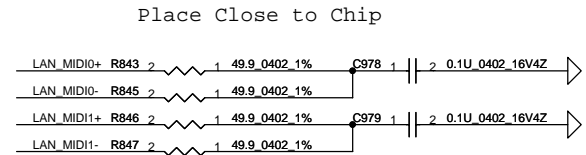
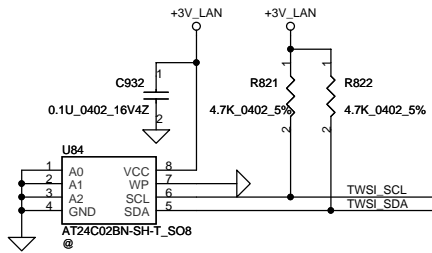
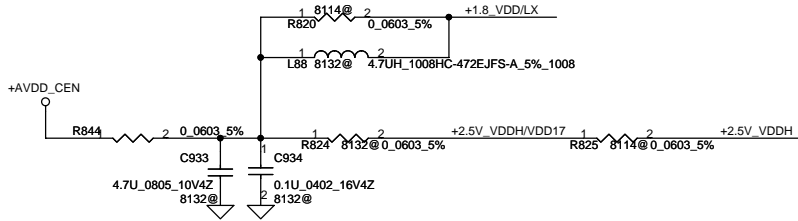
LCD/PANEL CONN.



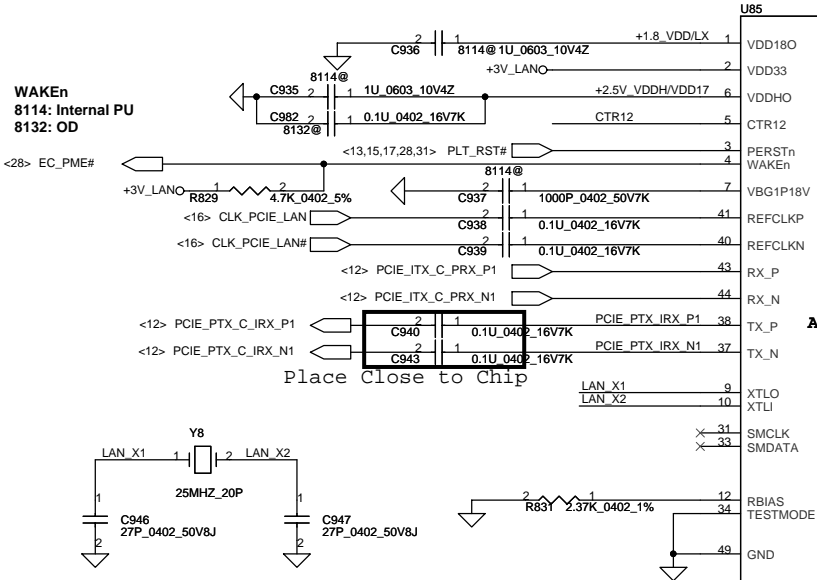
VARYBRIGHT FUNCTION



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				Document Number	C
				401743	
				Date: Wednesday, June 24, 2009	Sheet 24 of 47



WAKEn
8114: Internal PU
8132: OD

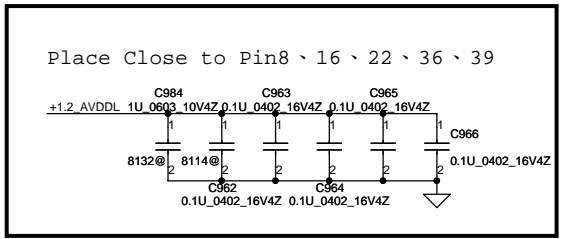
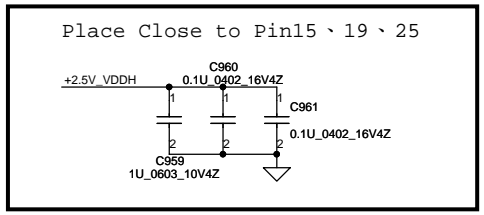
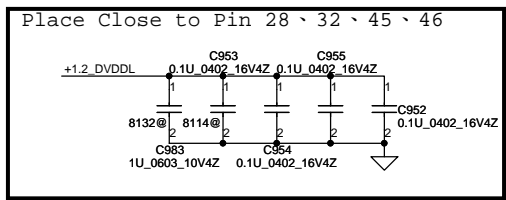
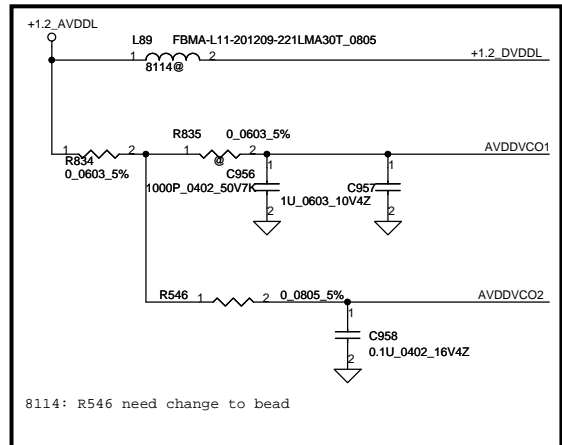
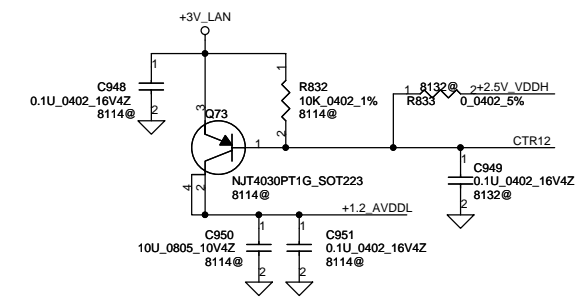
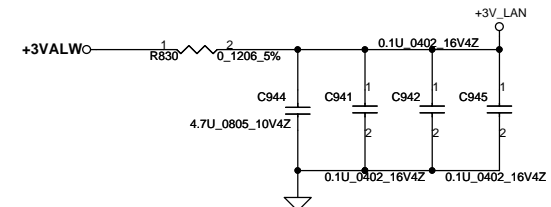


Atheros
AR8114A 10/100 LAN

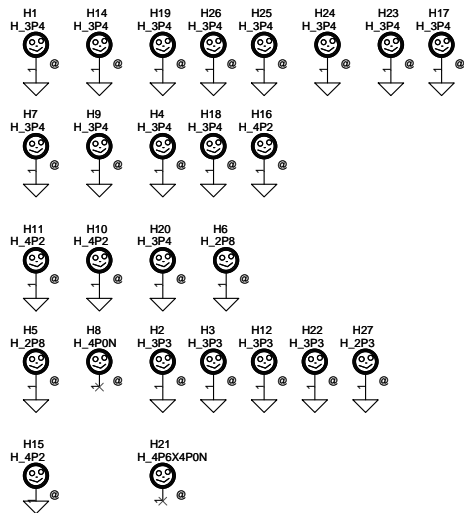
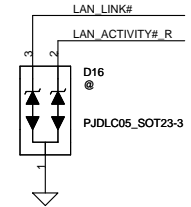
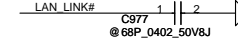
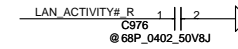
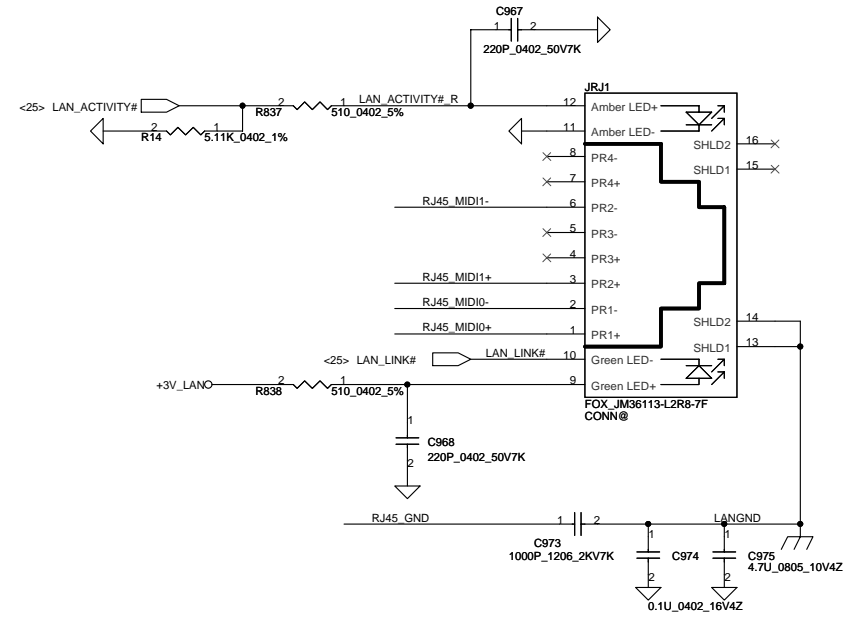
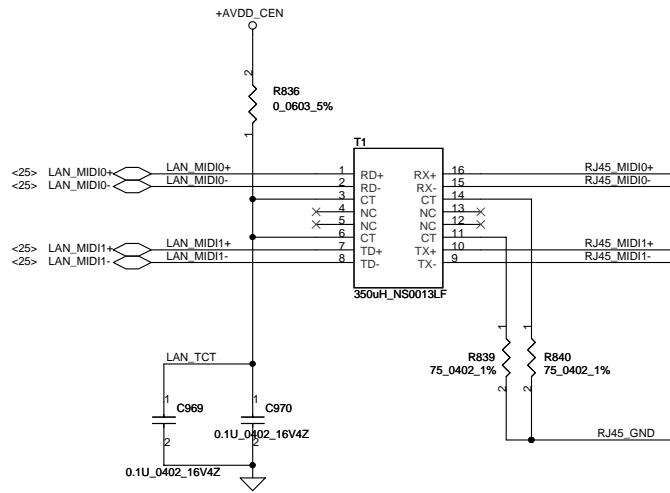
change to AR8132L-AL1E

Place Close to Chip

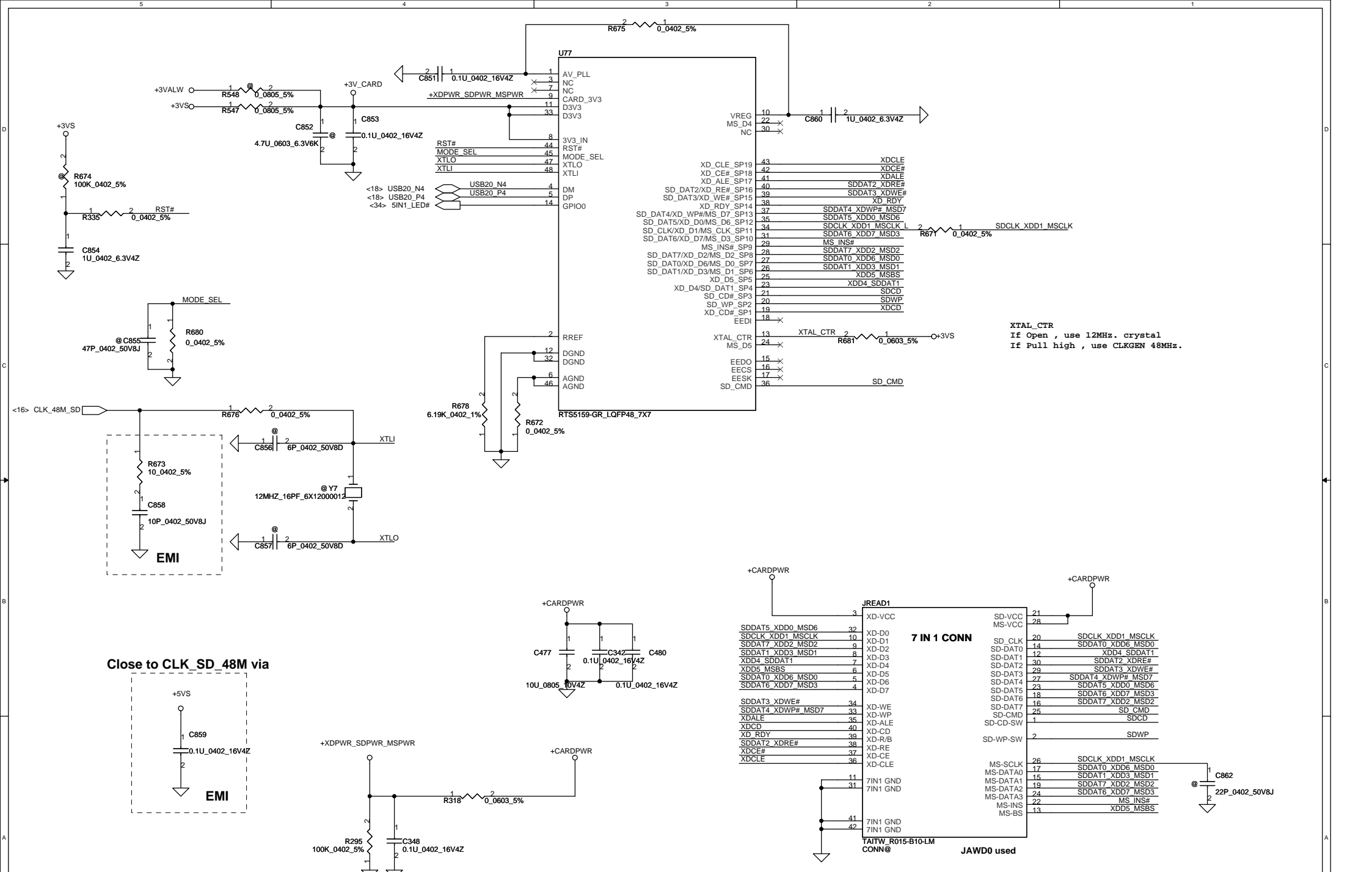
Layout Notice : Close to chip



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Size	B	Document Number	401743	Rev	C
Date:	Wednesday, June 24, 2009	Sheet	25	of	47



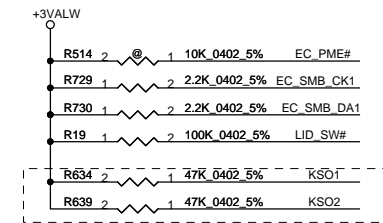
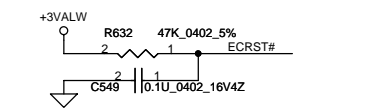
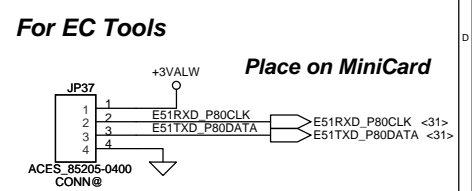
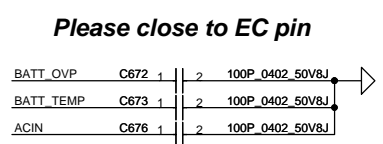
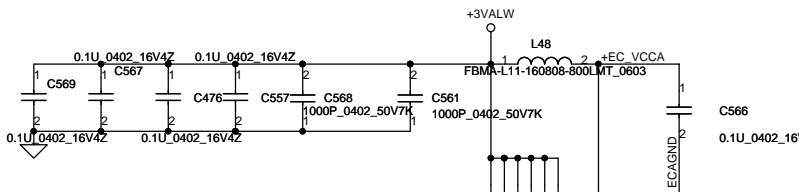
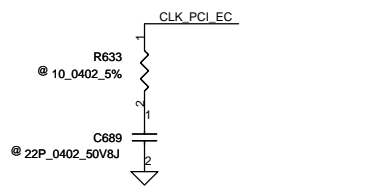
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				Custom	401743
				Date:	Wednesday, June 24, 2009
				Sheet	26 of 47
				Rev	C



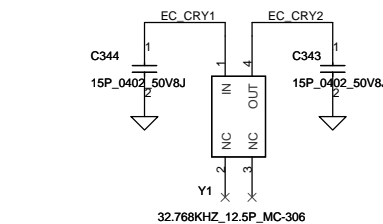
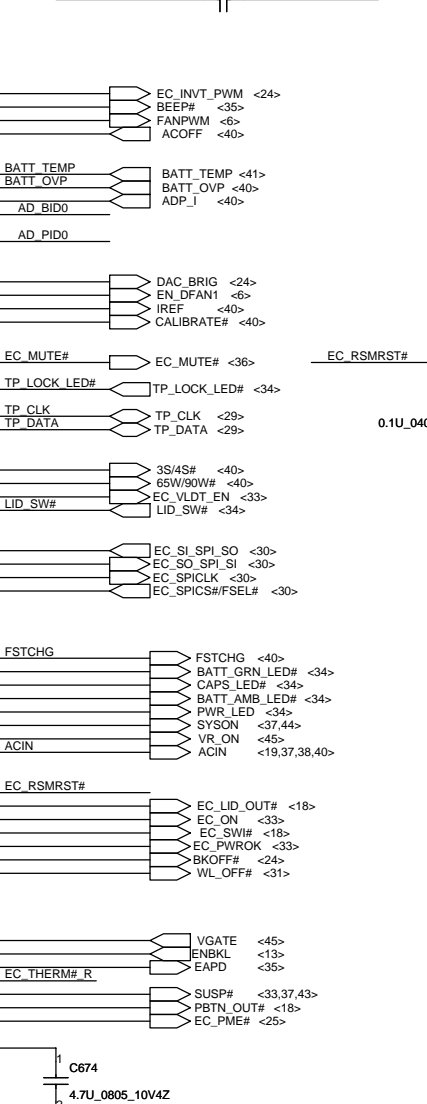
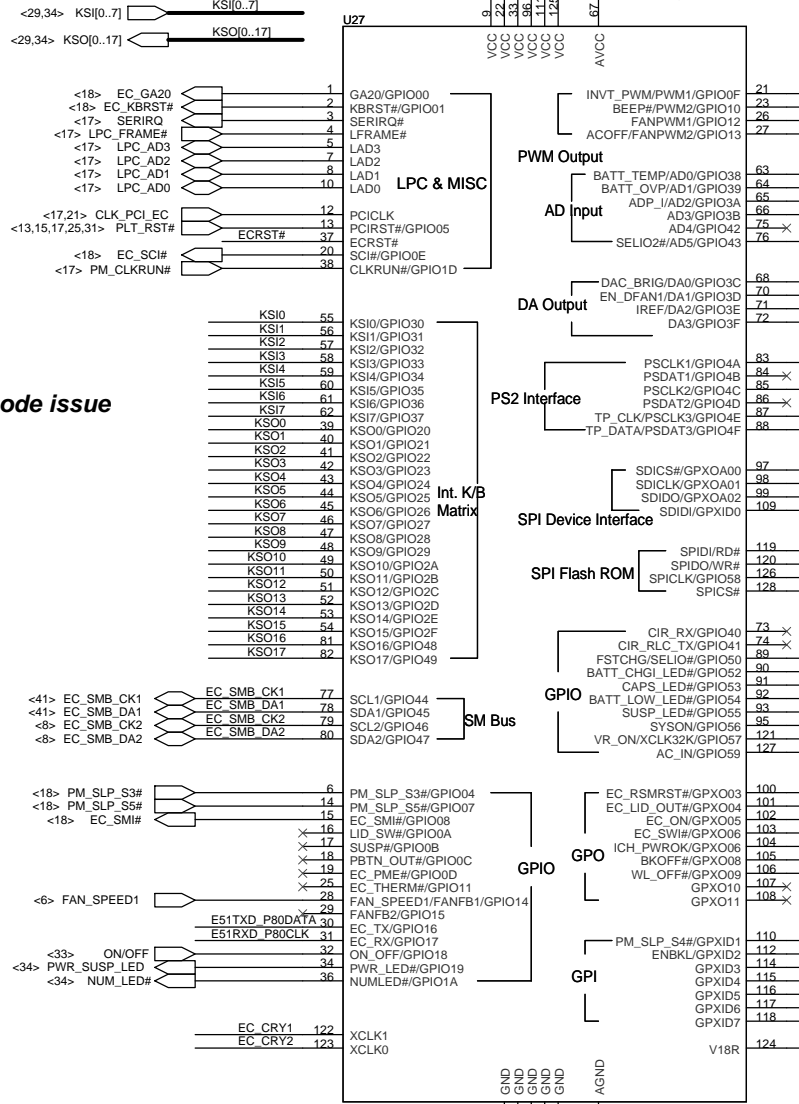
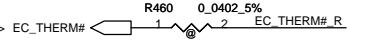
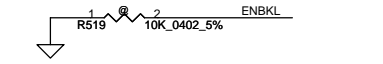
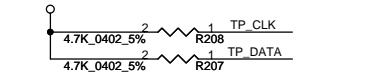
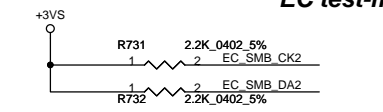
XTAL_CTR
 If Open, use 12MHz. crystal
 If Pull high, use CLKGEN 48MHz.

Close to CLK_SD 48M via

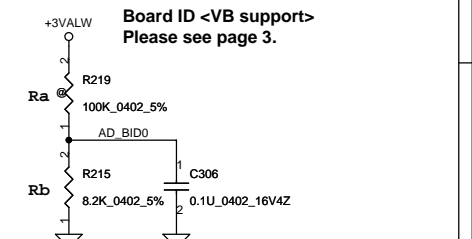
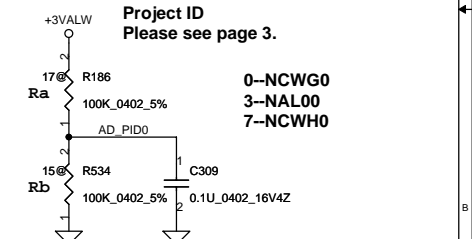
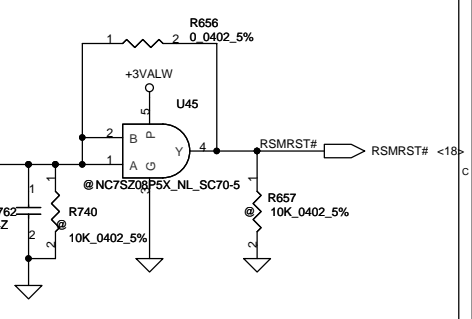
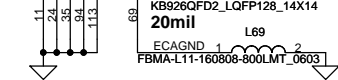
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2005/07/29		2010/03/12		401743	
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Date: Wednesday, June 24, 2009				Sheet 27 of 47	



EC test-mode issue

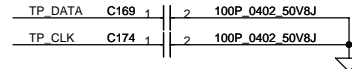
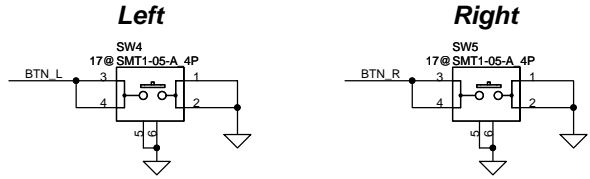


Chagne to D3 version

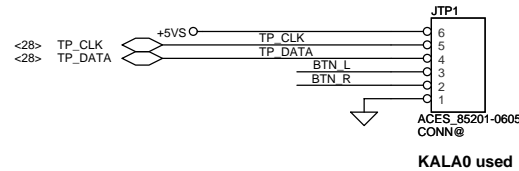


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				401743	C
				Date: Wednesday, June 24, 2009	Sheet 28 of 47

For 17"

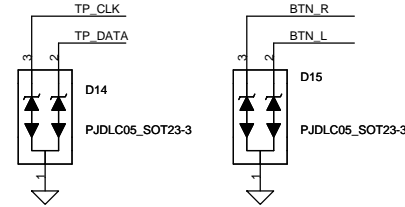
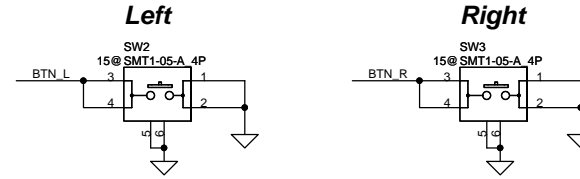


To TP/B Conn.

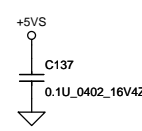


KALA0 used

For 15"



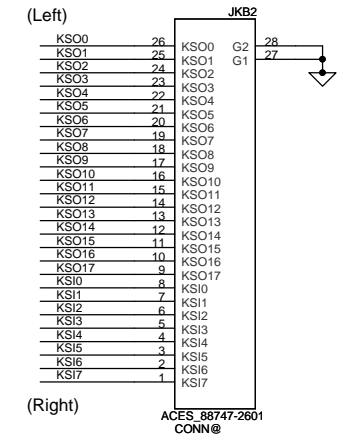
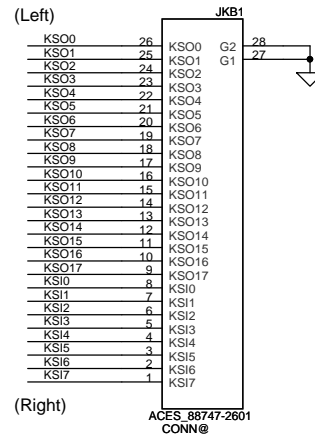
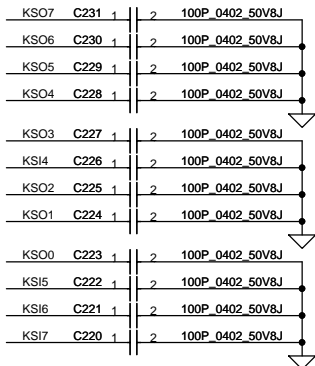
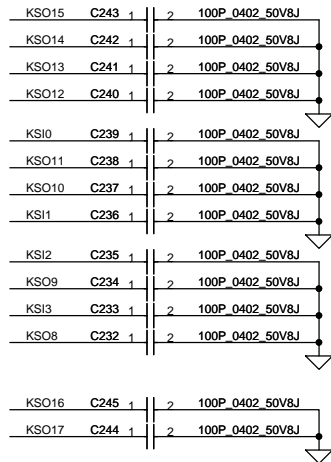
Change to SCA00000200



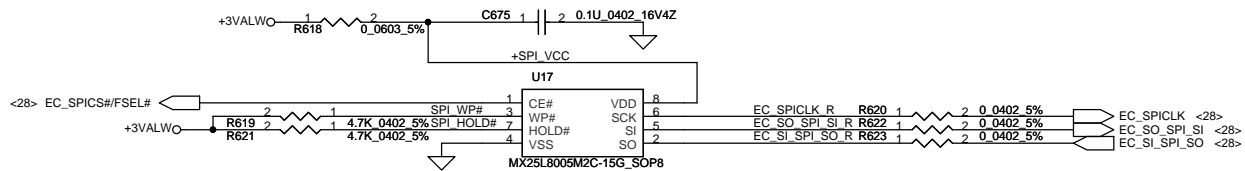
INT_KBD Conn.



KB1 for 15"
KB2 for 17"

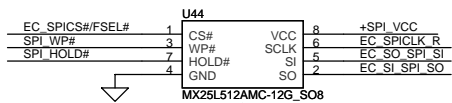
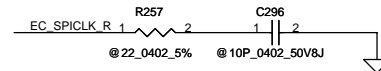


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Size Custom			Document Number	Rev C
			401743	
Date:		Wednesday, June 24, 2009	Sheet	29 of 47



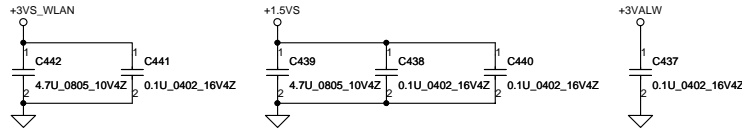
SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P
 ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

ONLY MXIC used in this project (66MHz)

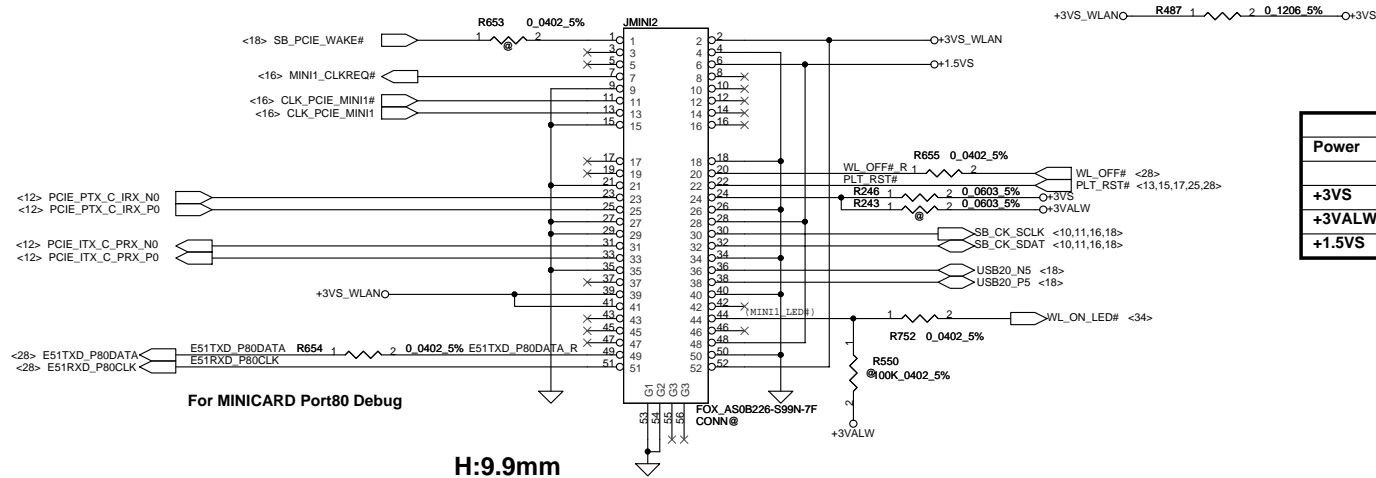


Reserved for BIOS simulator.
 Footprint S08
SPI ROM Footprint 150mil

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			Size Custom	Document Number
				401743
			Date:	Wednesday, June 24, 2009
			Sheet	30 of 47
			Rev	C



For Wireless LAN



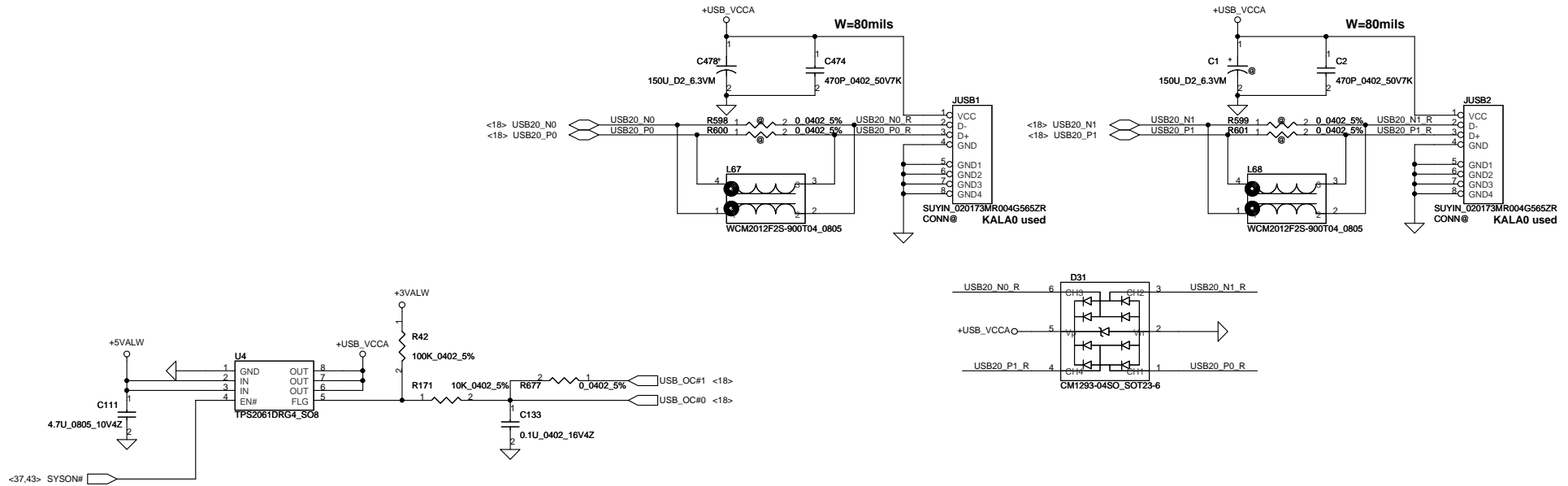
For MINICARD Port80 Debug

H:9.9mm

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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				Date:	Wednesday, June 24, 2009	Sheet 31 of 47

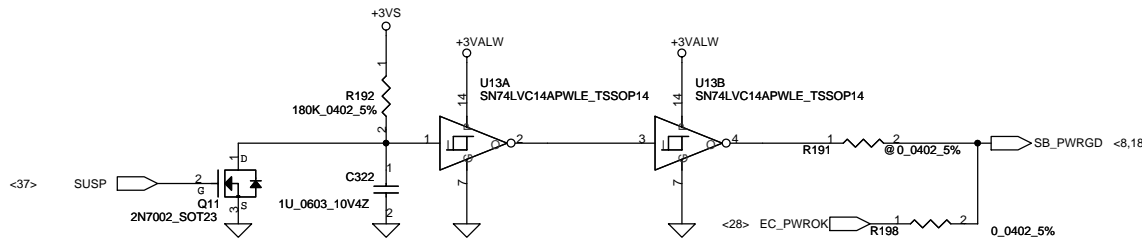
USB CONN. 1 & 2



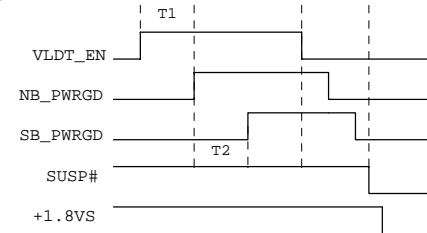
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				Date:	Wednesday, June 24, 2009	Sheet 32 of 47

Power ON Circuit

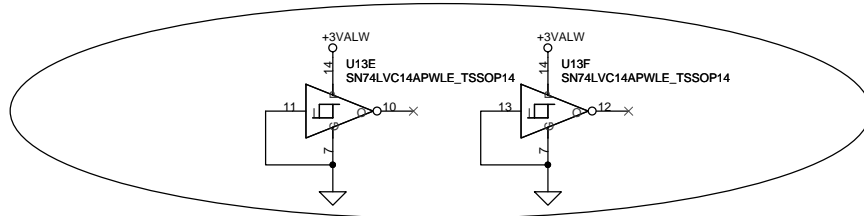
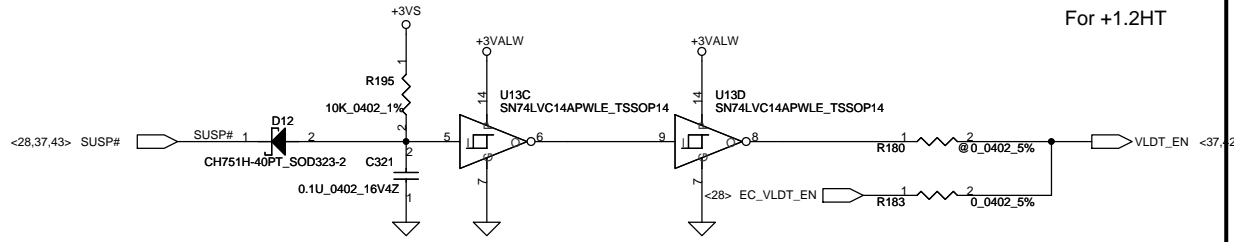
For South Bridge



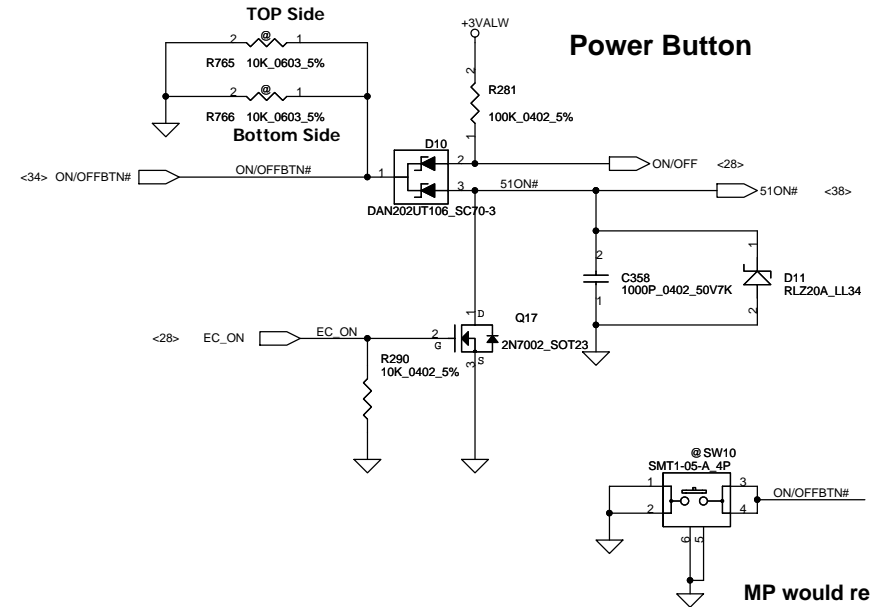
note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



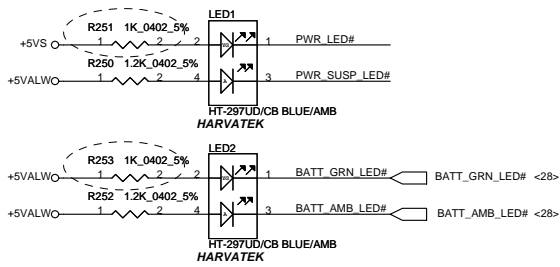
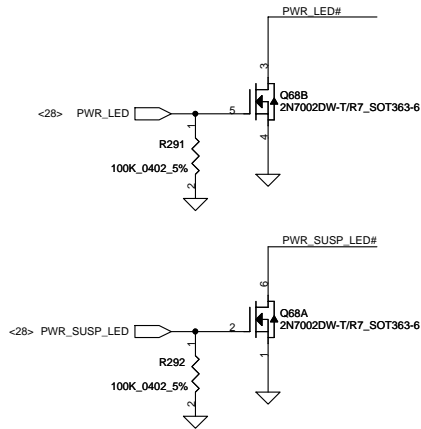
For +1.2HT



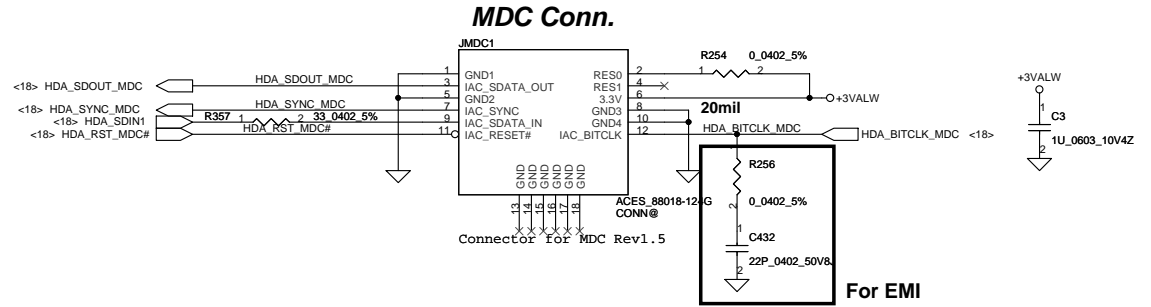
Power Button



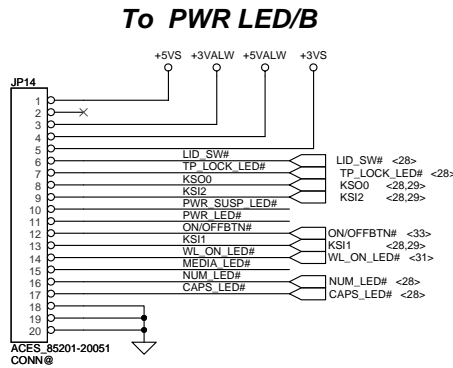
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				B	401743
				Date:	Wednesday, June 24, 2009
				Sheet	33 of 47
				Rev	C



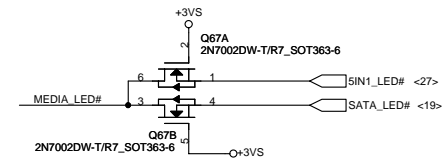
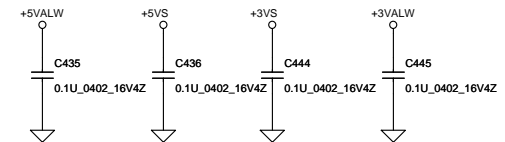
BLUE/AMB LED



For EMI

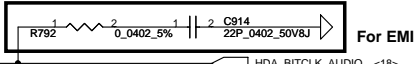
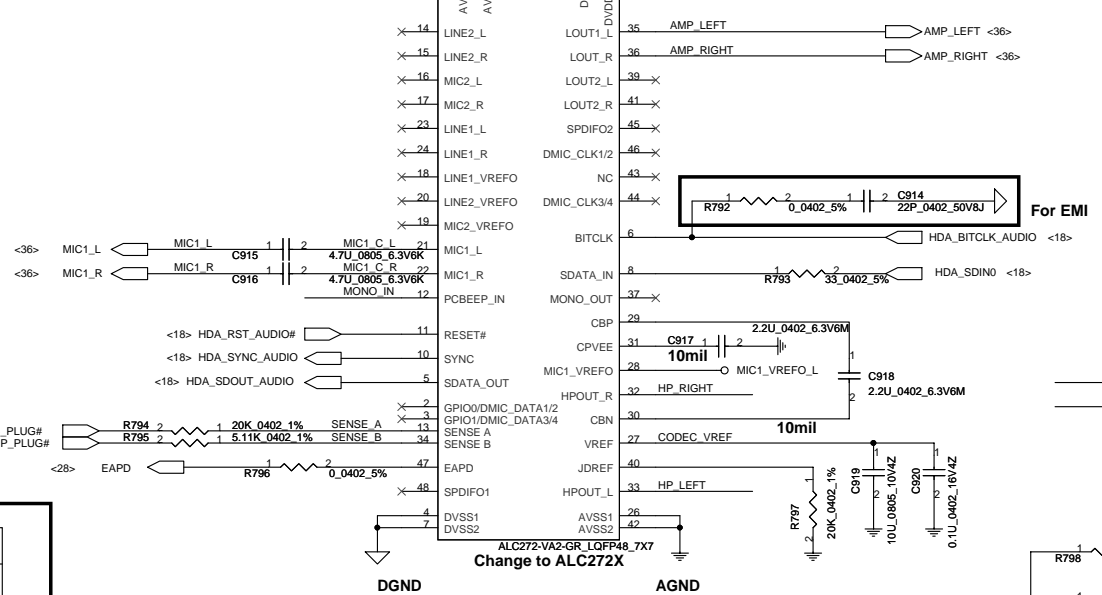
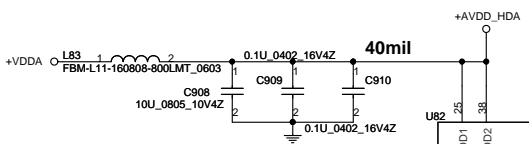
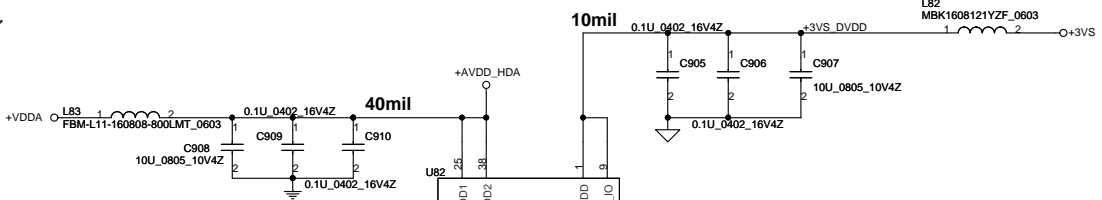
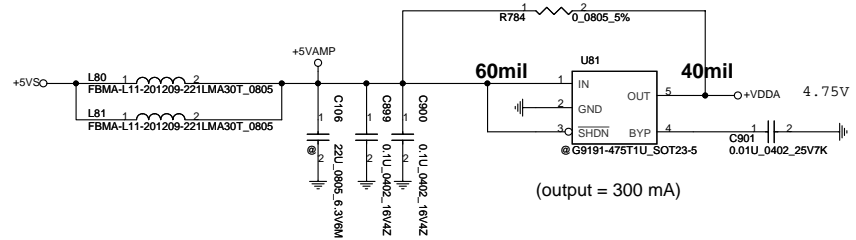
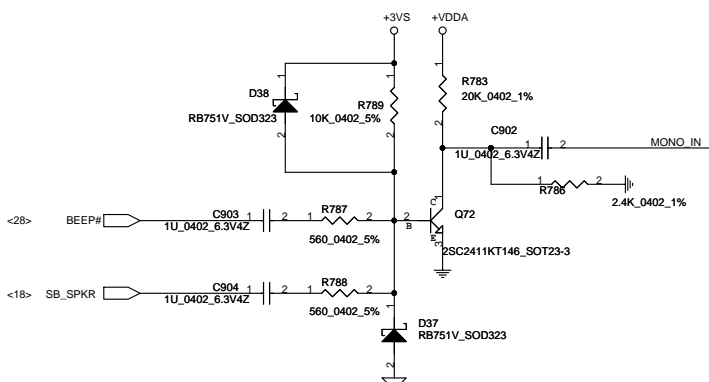


	KSO0
KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



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				Date:	Wednesday, June 24, 2009
				Sheet	34 of 47
				Rev	C

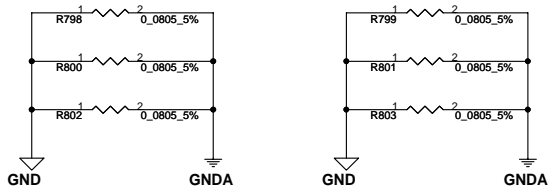
HD Audio Codec



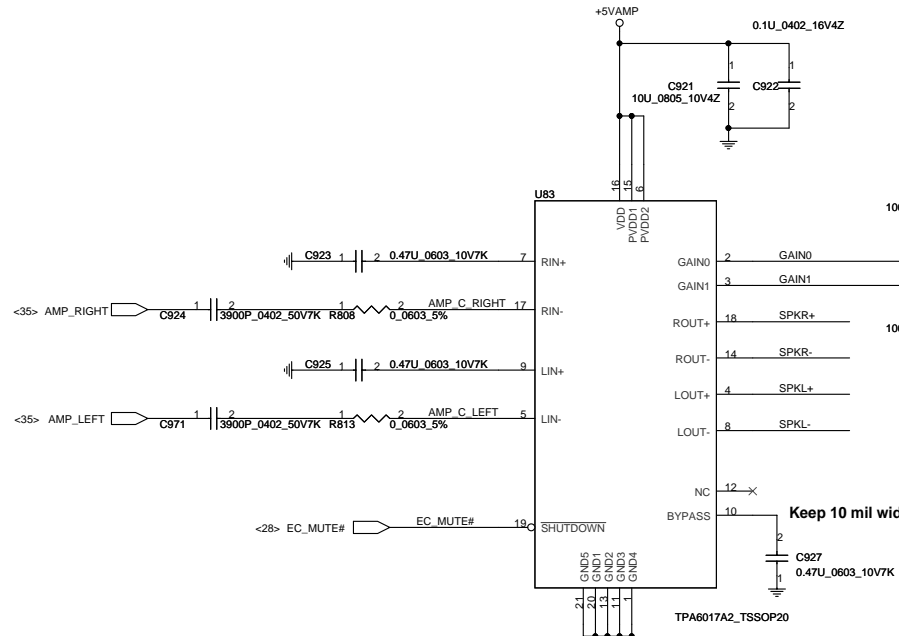
For EMI

update this table

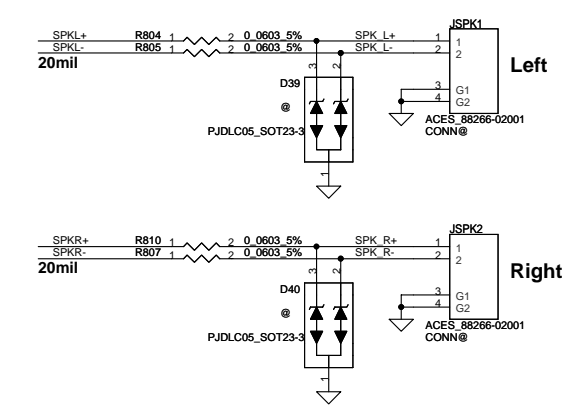
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



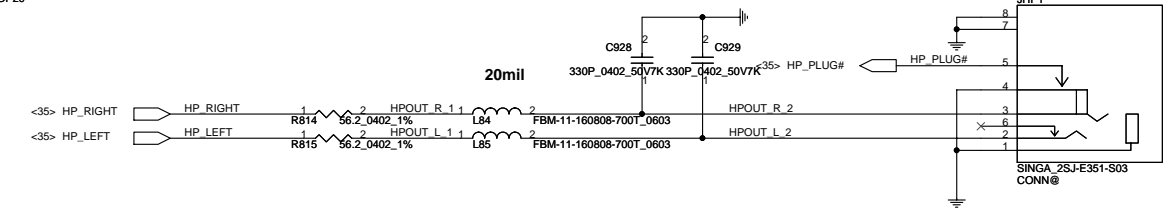
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Date: Wednesday, June 24, 2009				Sheet	35 of 47



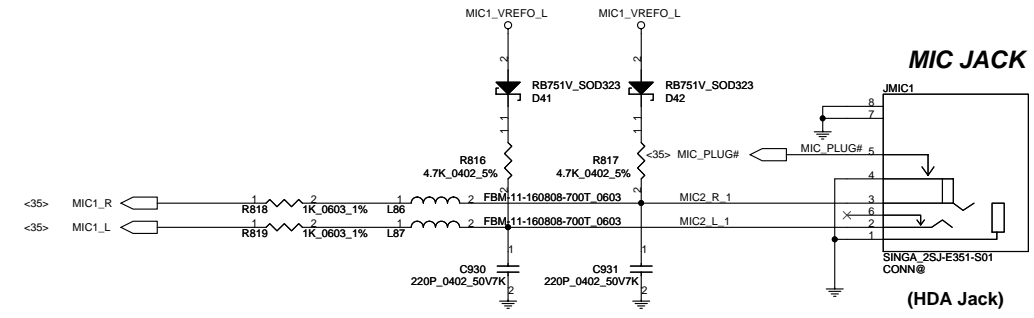
Int. Speaker Conn.



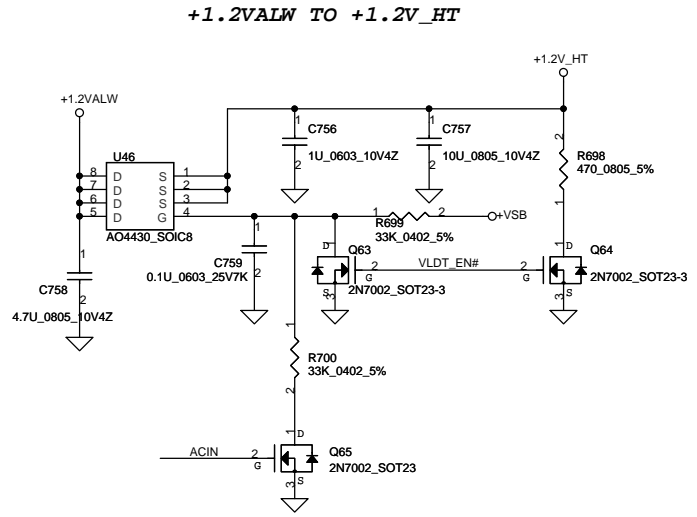
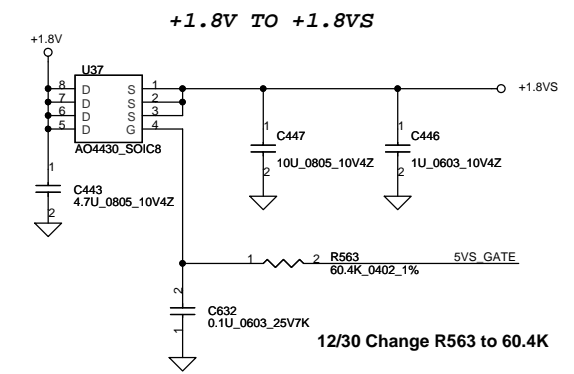
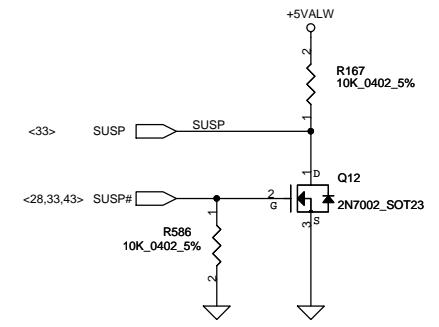
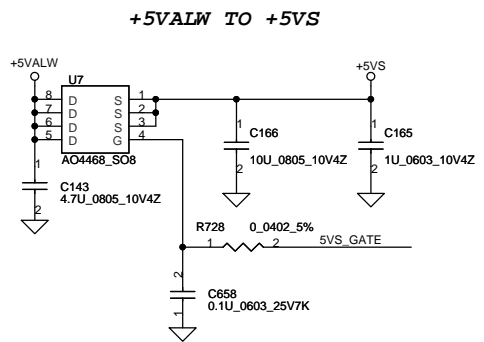
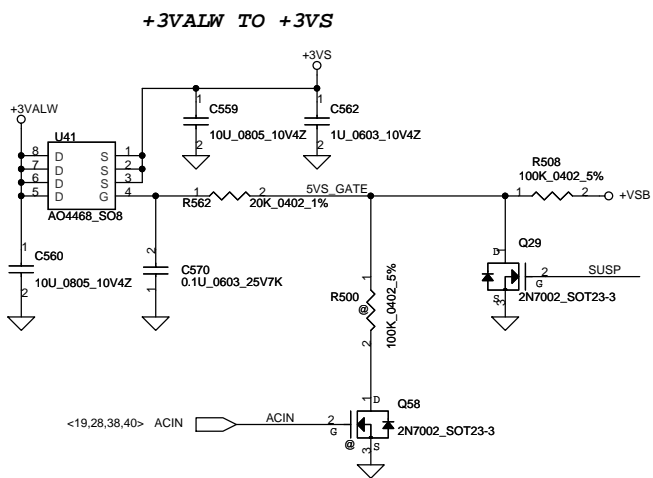
LINE Out/Headphone Out



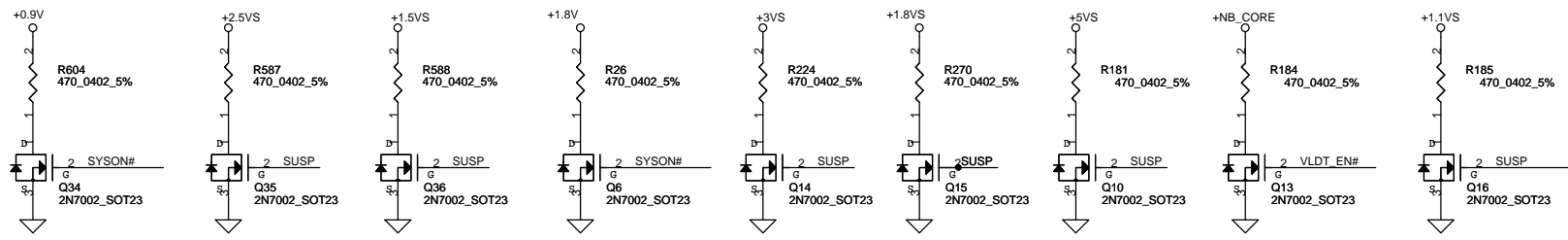
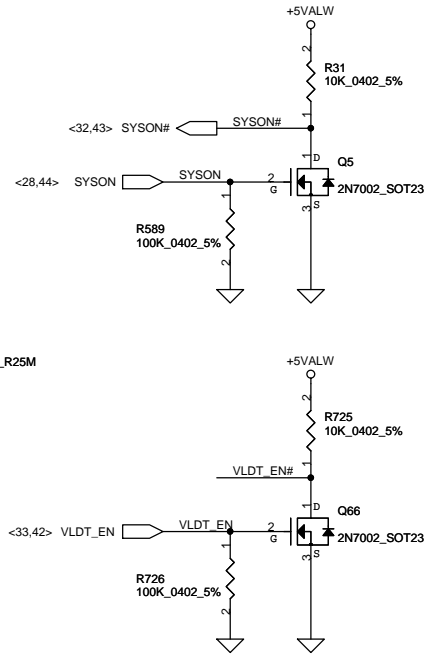
MIC JACK



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				401743	C
Date: Wednesday, June 24, 2009				Sheet	36 of 47

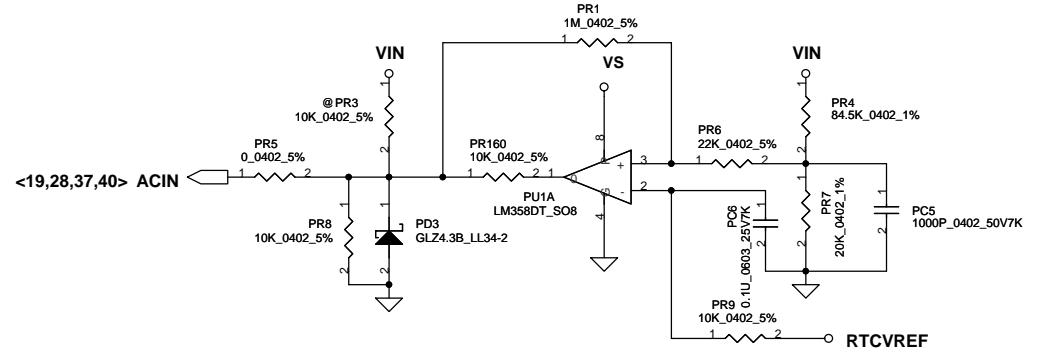
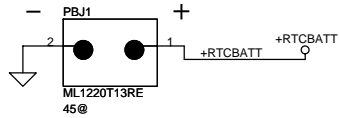
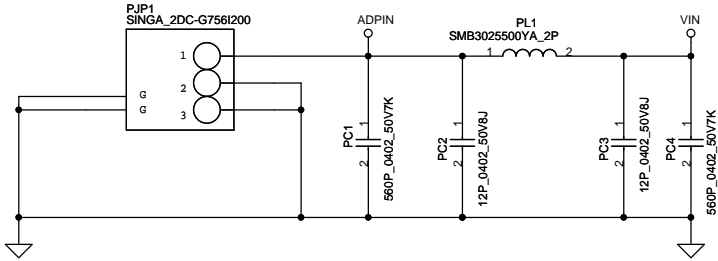


+1.2VALW
C30 220U_B2_2.5VM_R25M
For PWR request

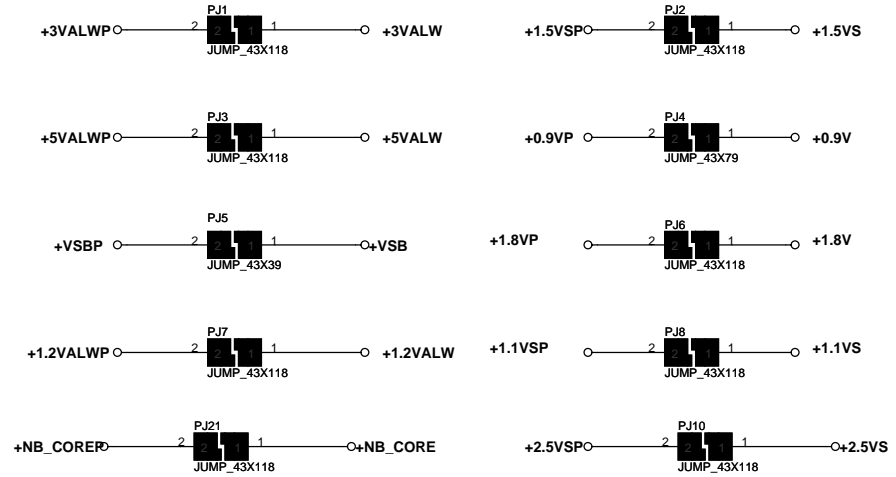
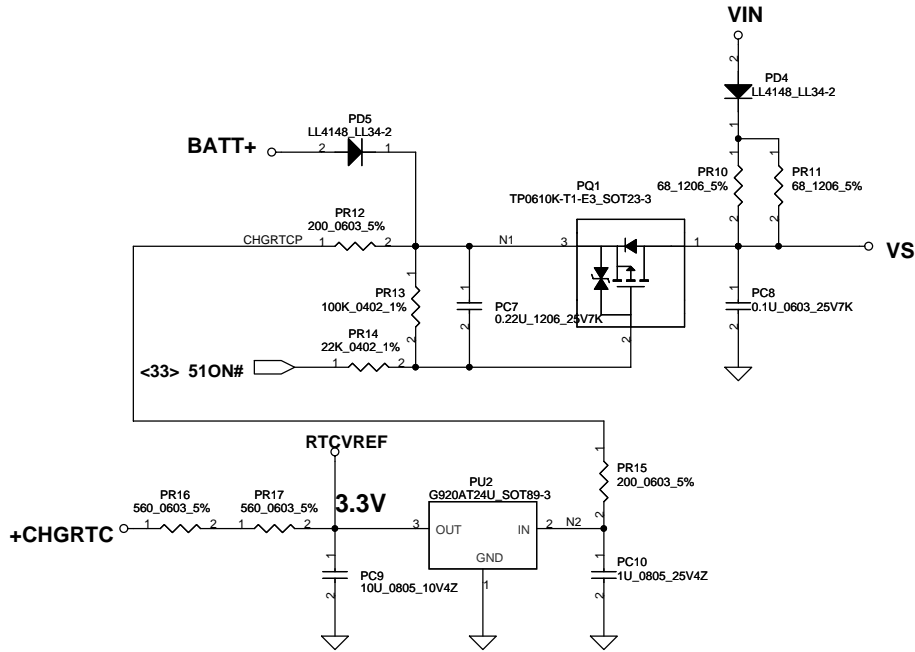


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				401743	C
Date: Wednesday, June 24, 2009				Sheet	37 of 47

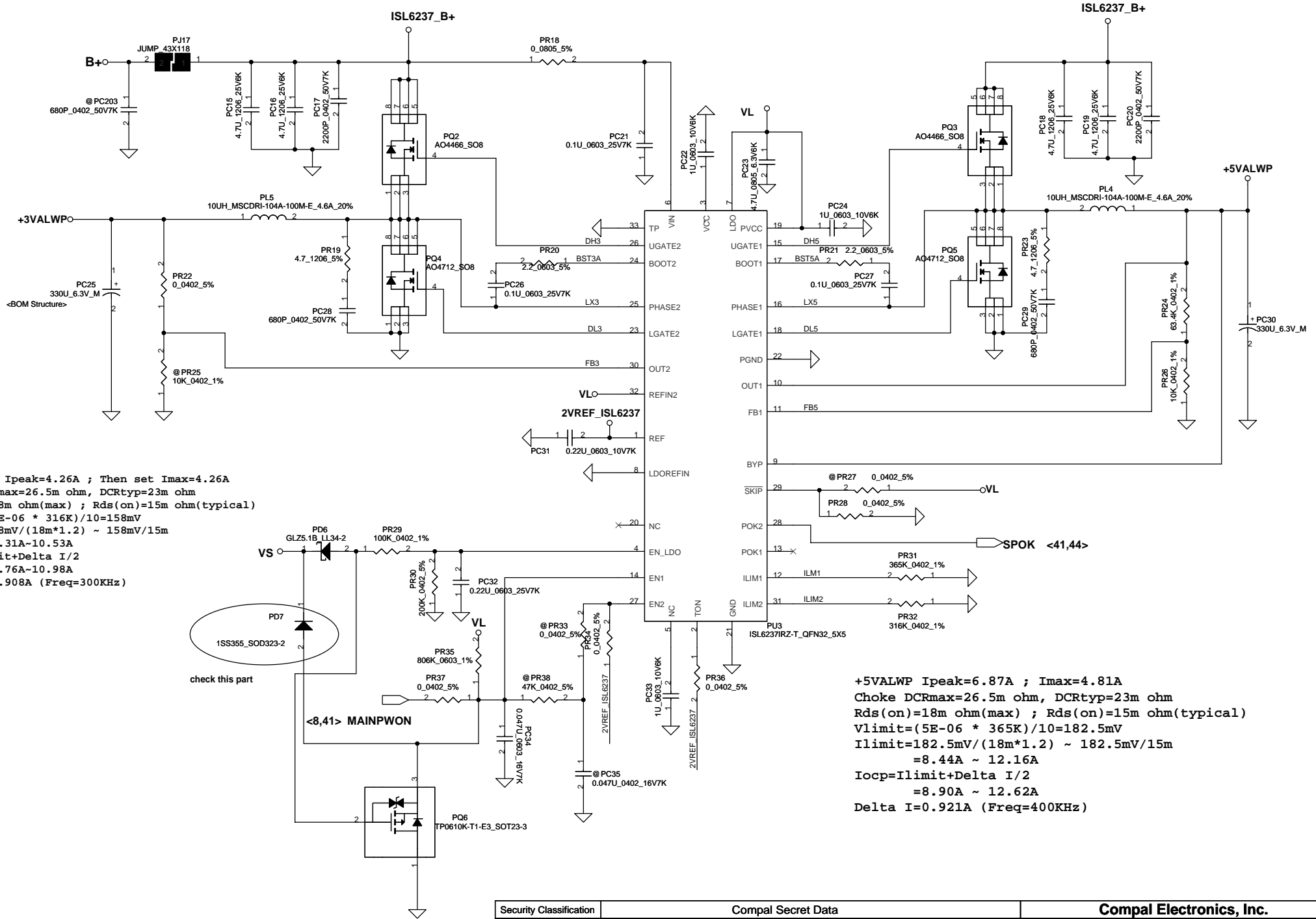
DC231000500



Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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				Date:	Wednesday, June 24, 2009	Sheet 38 of 47

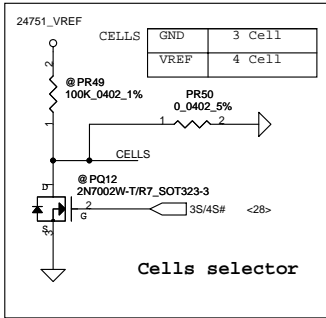
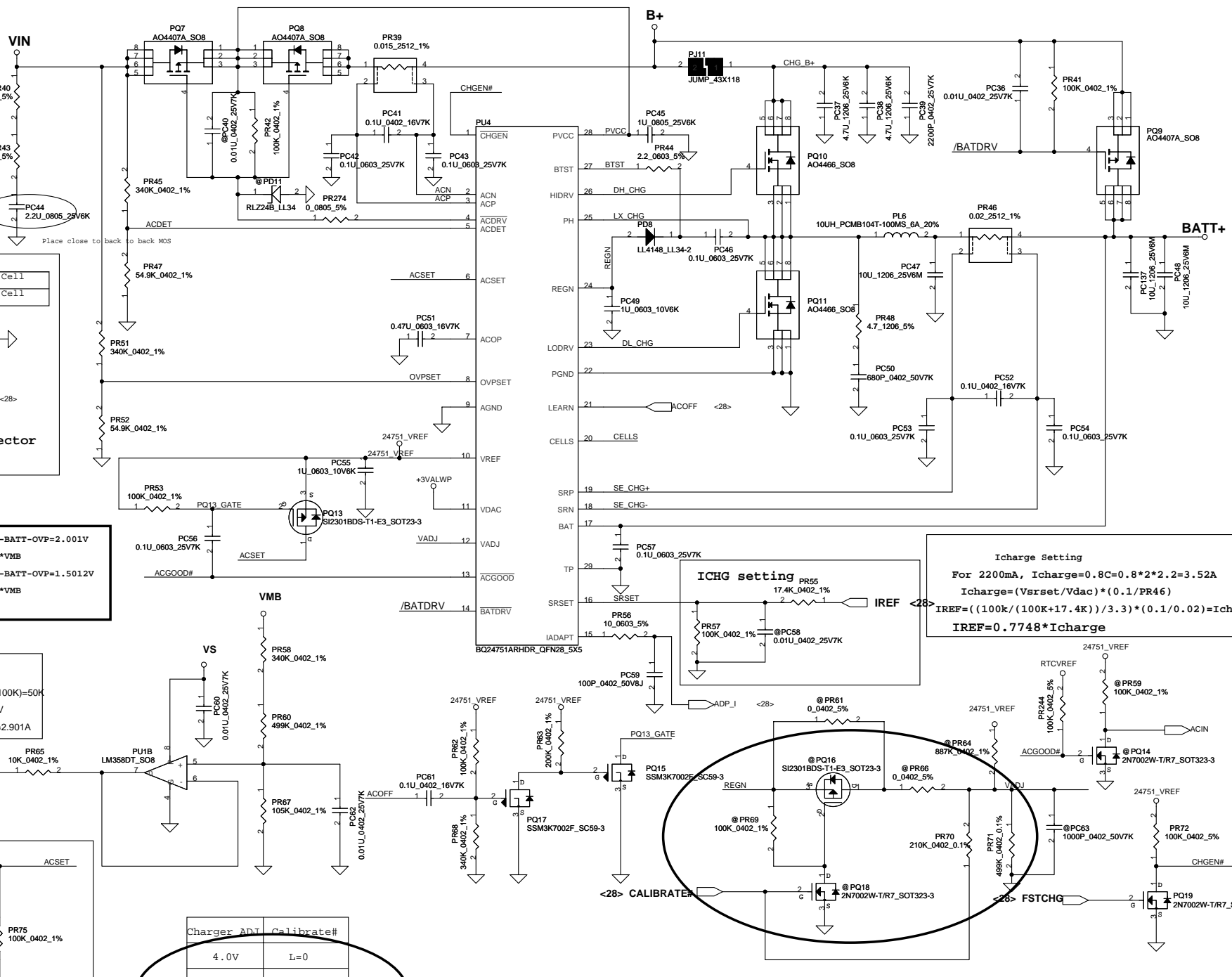


+3.3VALWP Ipeak=4.26A ; Then set I_{max}=4.26A
 Choke DCR_{max}=26.5m ohm, DCR_{typ}=23m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 316K)/10=158mV
 I_{limit}=158mV/(18m*1.2) ~ 158mV/15m
 =7.31A~10.53A
 I_{ocp}=I_{limit}+Delta I/2
 =7.76A~10.98A
 Delta I=0.908A (Freq=300KHz)

+5VALWP Ipeak=6.87A ; I_{max}=4.81A
 Choke DCR_{max}=26.5m ohm, DCR_{typ}=23m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 V_{limit}=(5E-06 * 365K)/10=182.5mV
 I_{limit}=182.5mV/(18m*1.2) ~ 182.5mV/15m
 =8.44A ~ 12.16A
 I_{ocp}=I_{limit}+Delta I/2
 =8.90A ~ 12.62A
 Delta I=0.921A (Freq=400KHz)

check this part

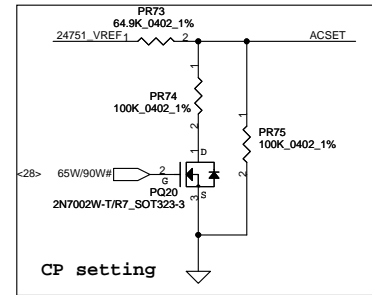
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Document Number	401743	Rev	C	Date:	Wednesday, June 24, 2009
Sheet	39	of	47		



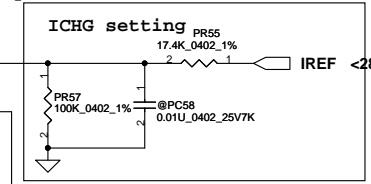
Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

LI-4S : 18.0V----BATT-OVP=2.001V
 BATT-OVP=0.1112*VMB
 LI-3S : 13.5V----BATT-OVP=1.5012V
 BATT-OVP=0.1112*VMB
 per cell=3.5V

CP Point Setting
 CP point=ladapter*85%
 65W adapter R=(100K*100K)/(100K+100K)=50K
 Vacset=3.3*(50K/(50K+64.9K))=1.436V
 CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A

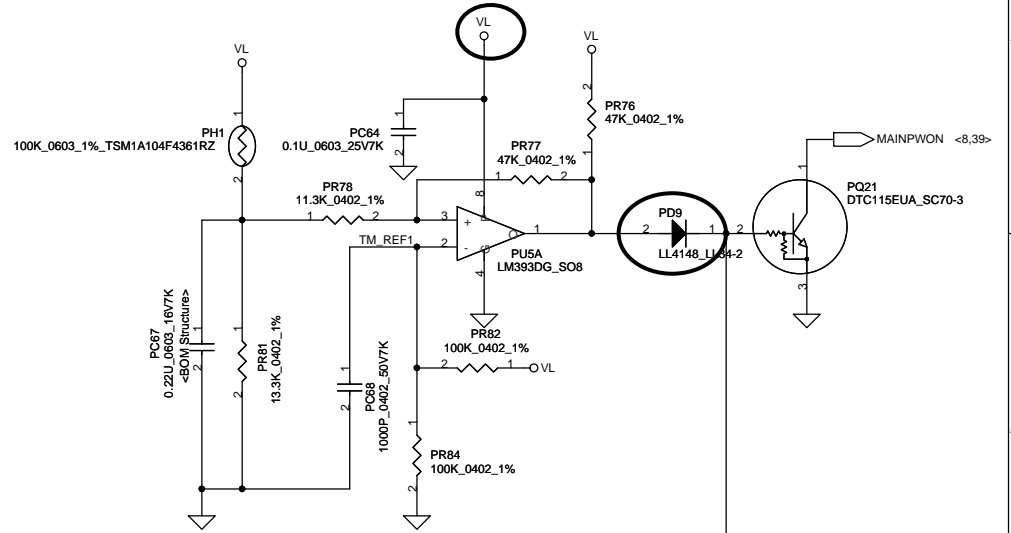


Charger ADI	Calibrate#
4.0V	L=0
4.2V	1.8755V
4.3V	2.8132V
4.35V	H=3.3V

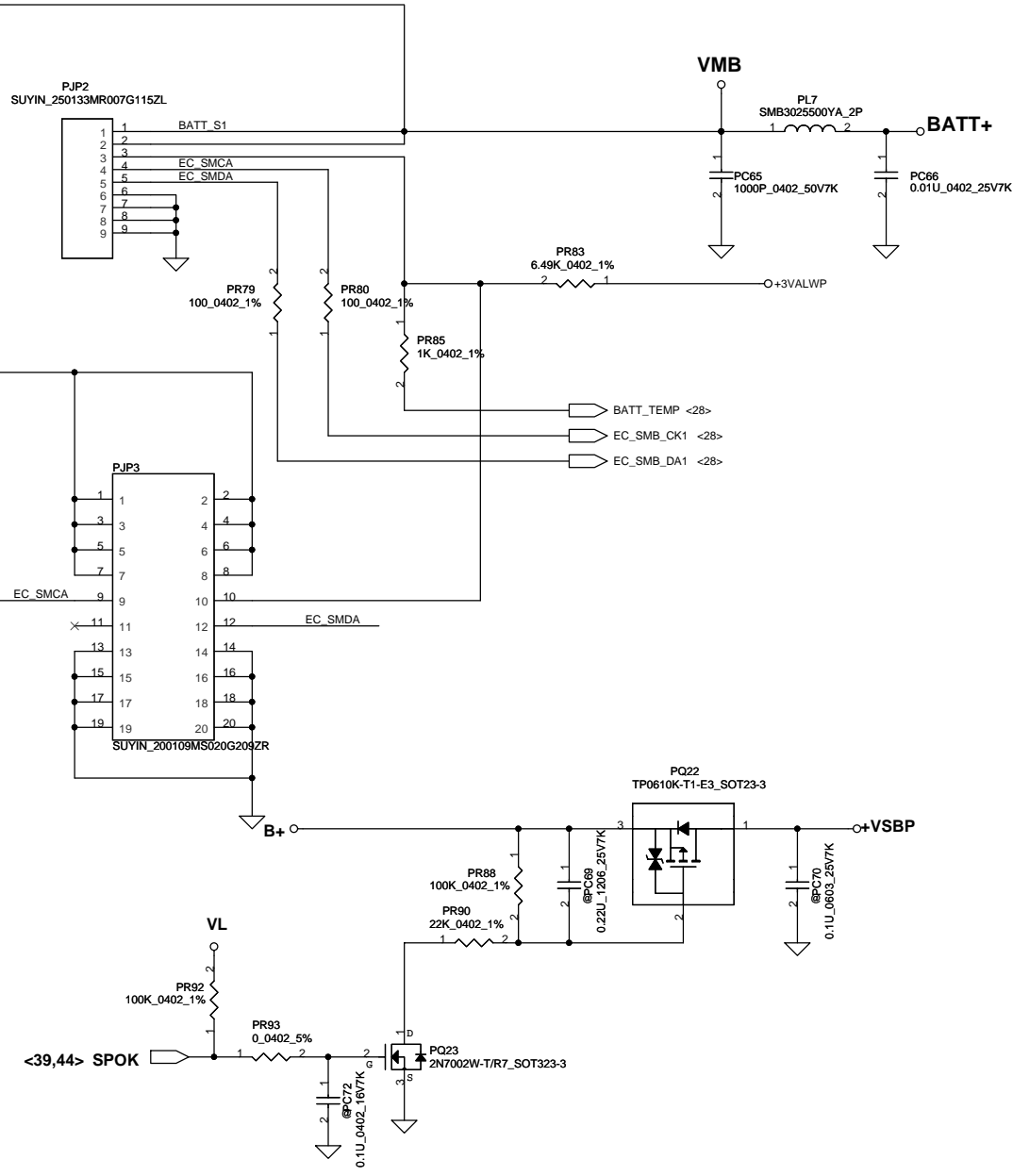
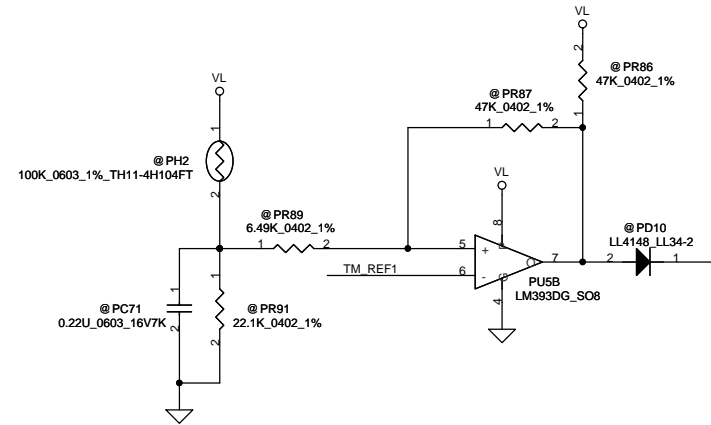


Icharge Setting
 For 2200mA, Icharge=0.8C=0.8*2*2.2=3.52A
 Icharge=(Vsrset/Vdac)*(0.1/PR46)
 $IREF = ((100k / (100k + 17.4k)) / 3.3) * (0.1 / 0.02) = Icharge$
 IREF=0.7748*Icharge

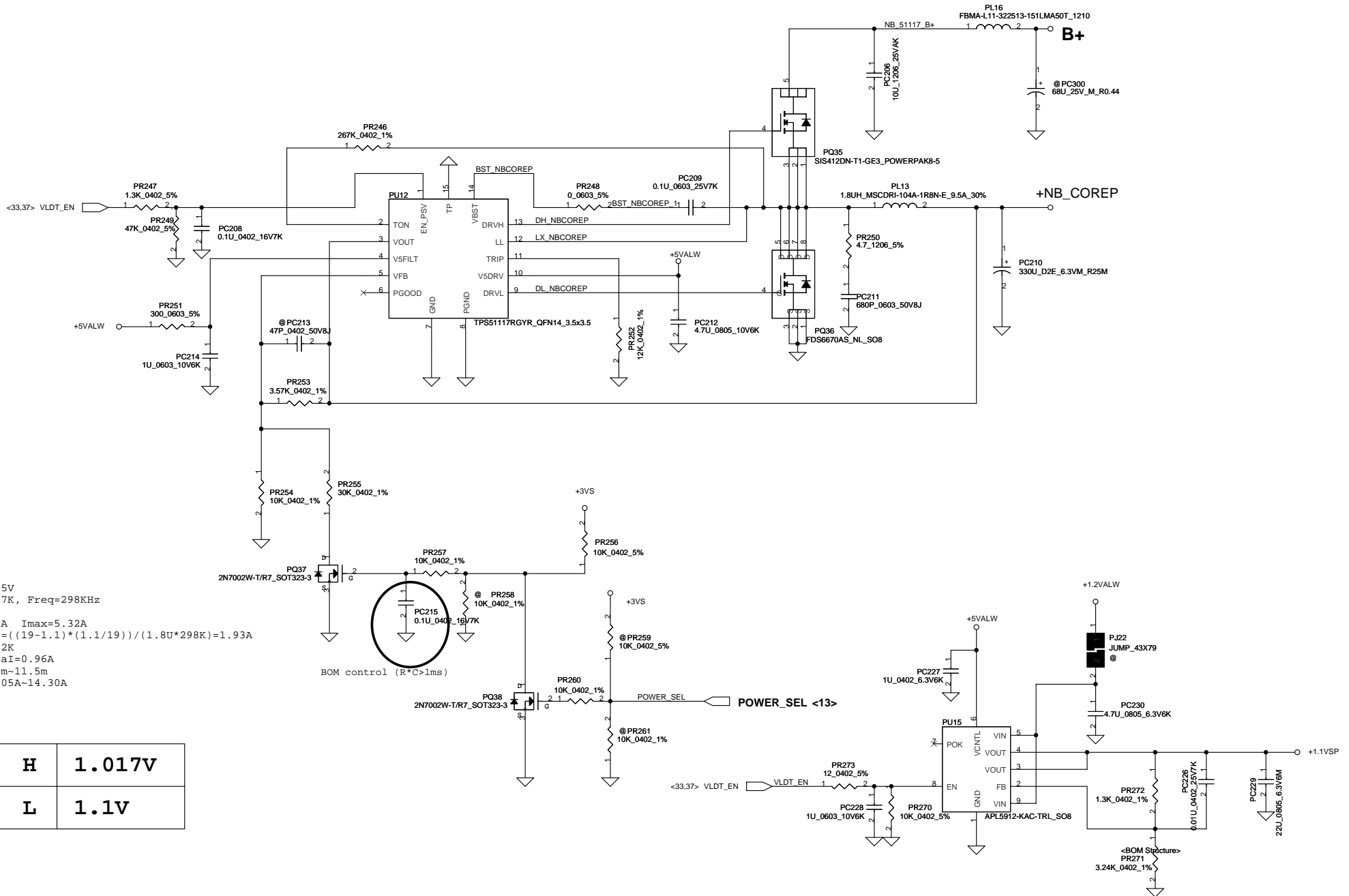
PH1 under CPU botten side :
CPU thermal protection at 92 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 75 degree C



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Size	Document Number	Rev			
B	401743	C			
Date:	Wednesday, June 24, 2009	Sheet	41	of	47

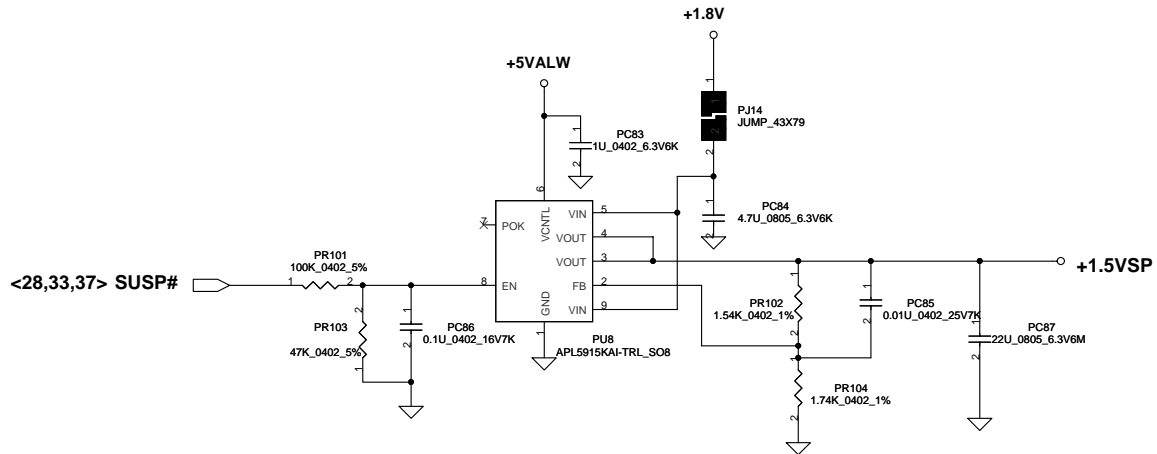
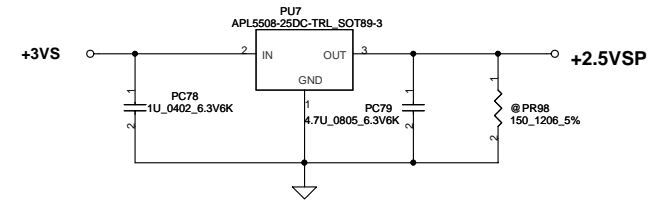
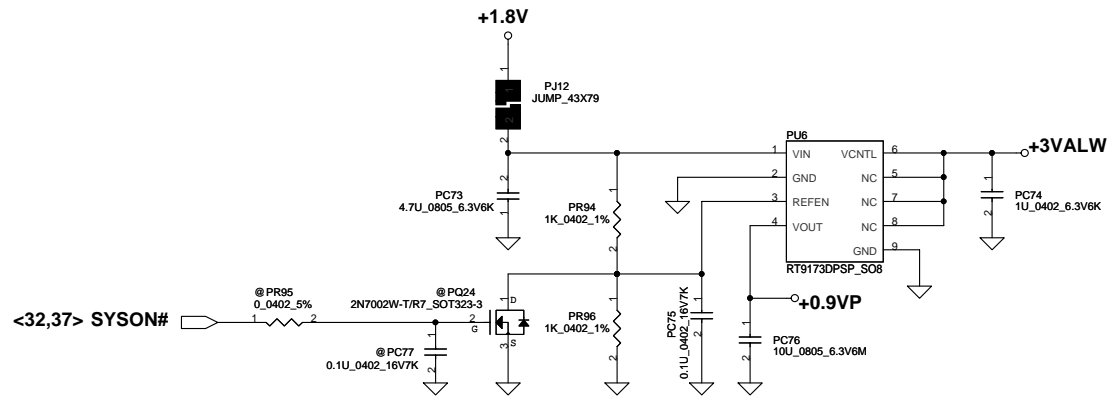


VFB=0.75V
 Rton=267K, Freq=298KHz
 Ipeak=7A Imax=5.32A
 $\Delta I = ((19-1.1) * (1.1/19)) / (1.8U * 298K) = 1.93A$
 Rtrip=12K
 $1/2 \Delta I = 0.96A$
 Rdson=9m~11.5m
 Iocp=9.05A~14.30A

BOM control (R*C>1ms)

H	1.017V
L	1.1V

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Date: Wednesday, June 24, 2009			Sheet	42	of 47



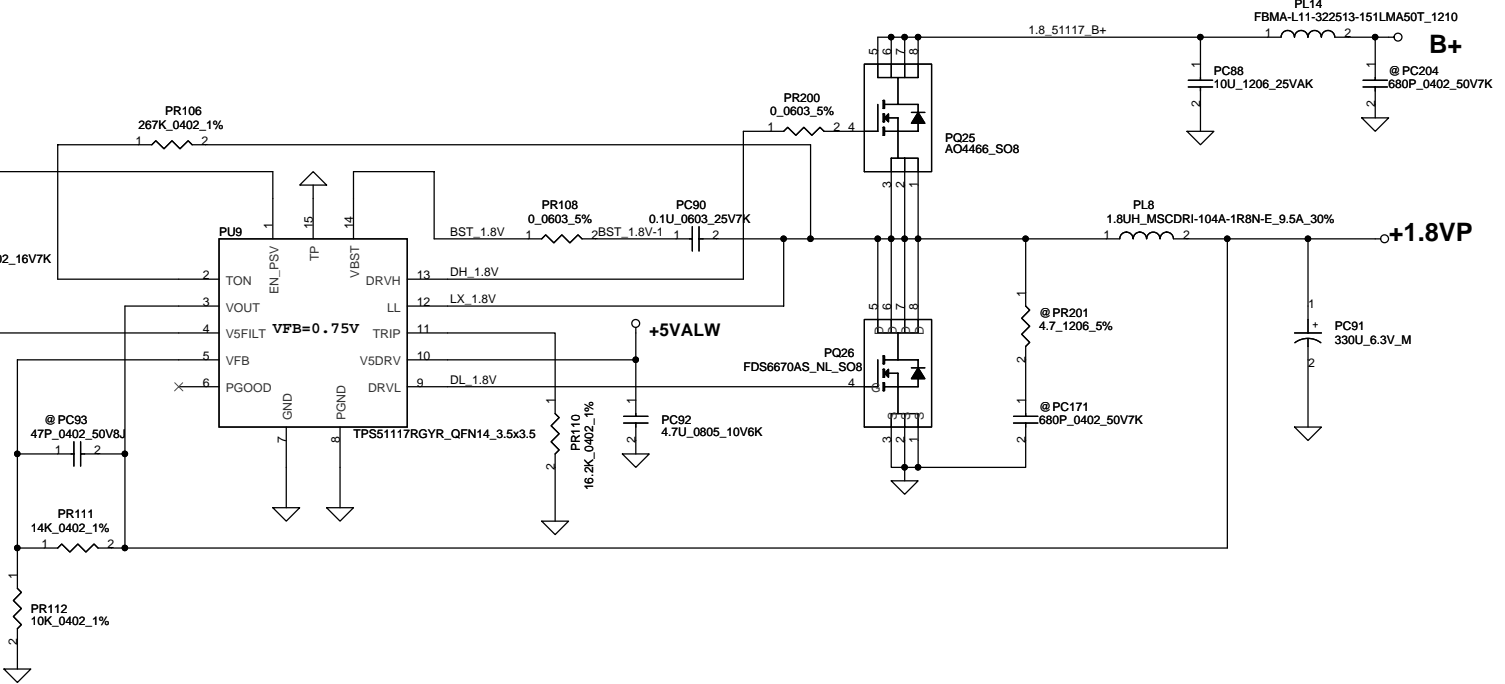
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Revision	401743	Document Number	401743	Rev	C
Date	Wednesday, June 24, 2009	Sheet	43	of	47

<28,37> SYSON

VFB=0.75V
 $V_o = VFB * (1 + PR111 / PR112) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 297KHz$

Cout ESR=15m ohm
 $I_{peak} = 11.96A, I_{max} = 8.372A$
 $\Delta I = ((19-1.8) * (1.8/19)) / (L * F_{sw})$
 $((19-1.8) * (1.8/19)) / (1.8u * 297000) = 3.048A$
 $\Rightarrow 1/2 \Delta I = 1.524A$

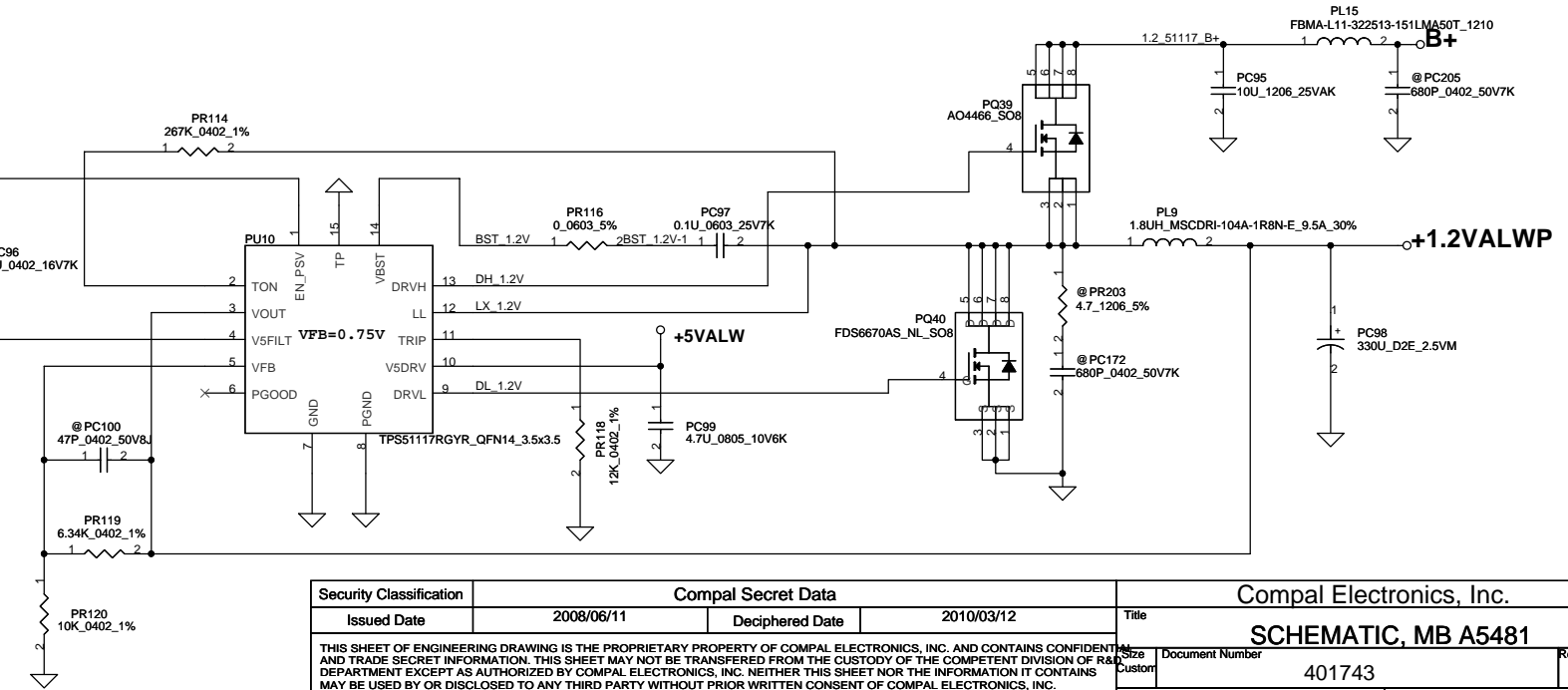
Rtrip=16.2K
 $I_{ocp} = 12.39A \sim 20.69A$



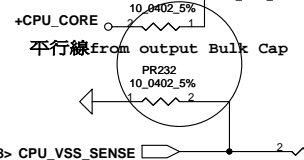
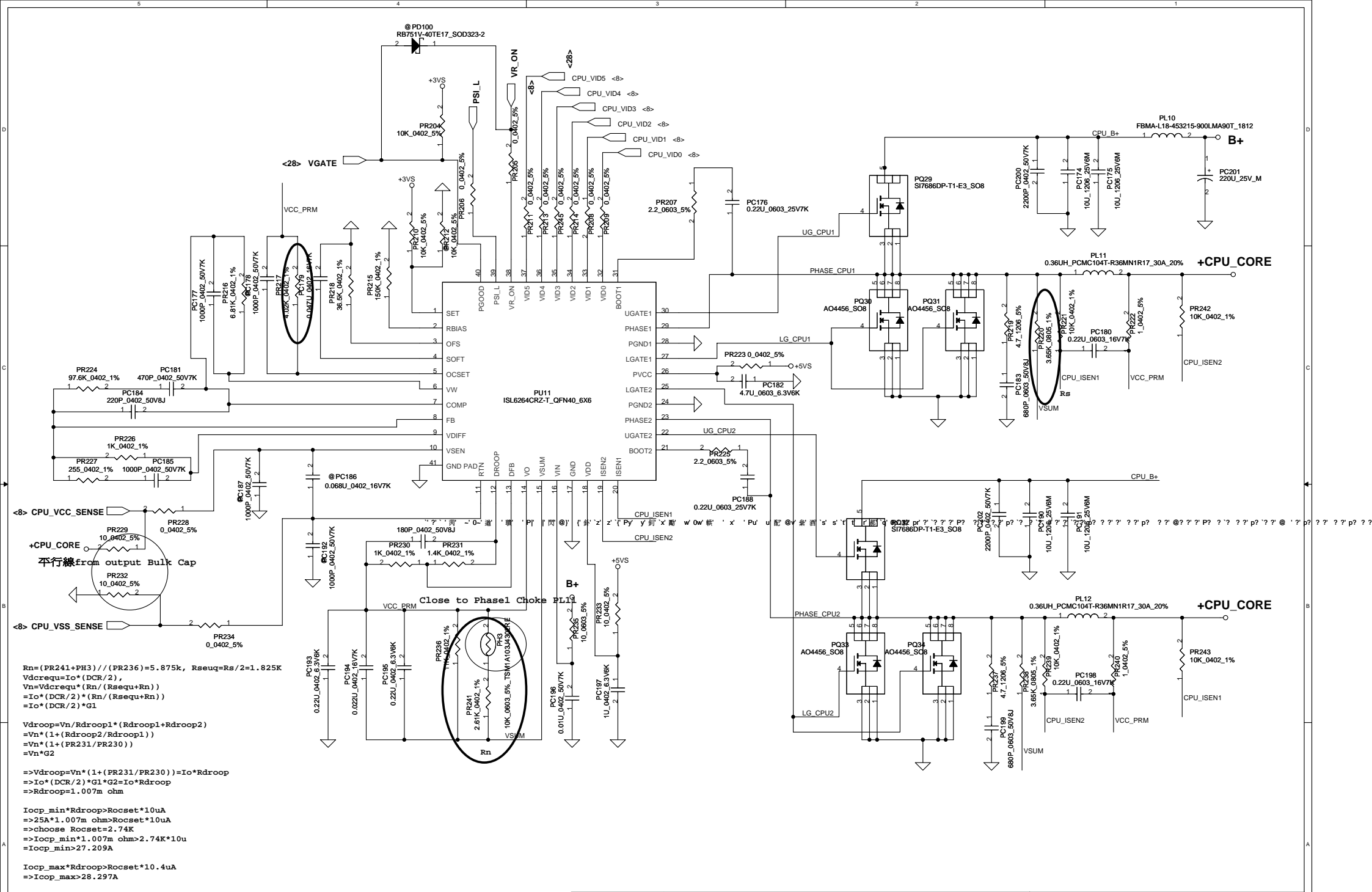
<39,41> SPOK

VFB=0.75V
 $V_o = VFB * (1 + PR119 / PR120) = 0.75 * (1 + 6.04K / 10K) = 1.203V$
 $R_{ton} = 267K \Rightarrow F_{sw} = 298KHz$

1.2VP Ipeak=7.4A ; Imax=5.180A
 $\Delta I = ((19-1.2) * (1.2/19)) / (L * F_{sw})$
 $((19-1.2) * (1.2/19)) / (1.8u * 298000) = 2.10A$
 $\Rightarrow 1/2 \Delta I = 1.05A$
 $R_{dson} = 11.5m / 9m \text{ ohm}$
 set Rtrip=12K
 $I_{ocp_min} = 9.11A$
 $I_{ocp_max} = 14.38A$



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Size	Document Number	Date	Sheet	of	Rev
Custom	401743	Wednesday, June 24, 2009	44	47	C



$R_n = (PR241 + PH3) / (PR236) = 5.875k$, $R_{sequ} = R_s / 2 = 1.825k$
 $V_{dcreq} = I_o * (DCR / 2)$
 $V_n = V_{dcreq} * (R_n / (R_{sequ} + R_n))$
 $I_o = I * (DCR / 2) * (R_n / (R_{sequ} + R_n))$
 $I_o = I * (DCR / 2) * G1$

$V_{droop} = V_n / R_{droop1} * (R_{droop1} + R_{droop2})$
 $= V_n * (1 + (R_{droop2} / R_{droop1}))$
 $= V_n * (1 + (PR231 / PR230))$
 $= V_n * G2$

$=> V_{droop} = V_n * (1 + (PR231 / PR230)) = I_o * R_{droop}$
 $=> I_o * (DCR / 2) * G1 * G2 = I_o * R_{droop}$
 $=> R_{droop} = 1.007m\ ohm$

$I_{ocp_min} * R_{droop} > R_{ocset} * 10\ \mu A$
 $=> 25A * 1.007m\ ohm > R_{ocset} * 10\ \mu A$
 $=> choose\ R_{ocset} = 2.74k$
 $=> I_{ocp_min} * 1.007m\ ohm > 2.74k * 10\ \mu A$
 $=> I_{ocp_min} > 27.209A$

$I_{ocp_max} * R_{droop} > R_{ocset} * 10.4\ \mu A$
 $=> I_{ocp_max} > 28.297A$

$I_{ocp} = -27.209A - 28.297A$

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Document Number	401743			Rev C
Date:	Wednesday, June 24, 2009	Sheet	45	of 47

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be gitter while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGA19331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
7							
8							
9							
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				Date:	Wednesday, June 24, 2009
				Sheet	46 of 46

Version change list (P.I.R. List) for HW

Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1	PWR update circuit			4/9	26				
2	BOM change	R118 reserve	P.18	4/9	27				
3	BOM change	Change R178, R179 to 90.9/158 ohm	P.16	4/9	28				
4	BOM change	R30, R39 reserve	P.24	4/9	29				
5	BOM change	Add C30	P.38	4/9	30				
6	BOM change	Add R634, R639	P.28	4/9	31				
7	BOM change	C383 Reserve	P.24	4/9	32				
8		Pop R419	P.20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1.D2 Reserve, pop R763	P.24	5/18					
11	For Panel flash issue	Add R414 and non-pop	P.24	5/18					
12	Lid_SW intial issue	Add R19	P.28	5/18					
13	HPET timer issue	Change C288,C290 to 33P	P.16	5/18					
14	BOM change	change C276,C279 10P to 27P	P.19	5/19					
15									
16									
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23									
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25									

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				401743	C
Date: Wednesday, June 24, 2009				Sheet	47 of 47